SSD1283A

Product Preview

132 RGB x 132 TFT Driver
Integrated Power, Gate, Source Driver with built-in RAM

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1 General Description

SSD1283A TFT Smart Driver is an all in one driver that integrated the power circuits, gate driver, source driver and RAM into single chip. It can drive a 262k color a-TFT panel with resolution of 132 RGB x 132.

It is also integrated with the controller function and consists of up to 39,204 bytes (132 x 132 x 18 / 8) Graphic Display Data RAM (GDDRAM), such that it interfaced with common MCU through 8/9/16/18-bits 6800-series / 8080-series compatible Parallel Interface or Serial Interface and stored the data in the GDDRAM. Auxiliary 18-bits video interface (VSYNC, HSYNC, DOTCLK, ENABLE and RR0-RR5, GG0-GG5, BB0-BB5) are integrated into SSD1283A for displays animated image.

With 9 external capacitors only, it embeds DC-DC Converter, Oscillator and Voltage generator to provide all necessary voltage required by the driver with minimum external components. A Common Voltage Generation Circuit is included to drive the TFT-display counter electrode. An Integrated Gamma Control Circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

It can be operated down to 1.16V and provide different power save modes. It is suitable for any portable battery-driven applications requiring long operation period with compact size.

2 FEATURES

- Power Supply: V_{DD} = 1.65 V – 2.5V (non-regulated input for logic)
  V_{DDIO} = 1.4 V – 3.6V (regulated input for logic)
  V_{DDEXT} = 1.65 V – 3.6V (auxiliary input for logic when V_{DDIO} < 1.65 V)
  V_{CI} = 2.5V – 3.6V (power supply for internal analog circuit)
- Maximum Gate Driving Output Voltage : 30V p-p
- Source Driving Output Voltage: 0-5V
- Low Current Sleep Mode, Partial Display Mode and 8-colors mode for power saving
- Display Size: 132 RGB x 132
- Display Color Support: 262k/65k colors a-TFT displays
- 8/9/16/18-bits 6800-series / 8080-series Parallel Interface, Serial Peripheral Interface
- 18-bit RGB-Interface for animated displays (VSYNC, HSYNC, DOTCLK, DEN, and PD0-17)
- On-Chip 39,204 bytes (132x132x18/8) Graphic Display Data RAM
- Support Line and Frame Inversion
- Source and Gate scan direction control
- Software selection on Center Screen Scrolling, Top Screen Scrolling, Bottom Screen Scrolling and Whole Screen Scrolling
- On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
- On-Chip DC-DC Converter up to 6x / -6x
- Typical Source Output Voltage variation: ±10 mV
- Programmable Common Electrode Voltage amplitude and level for both Cs on gate or Cs on common structure
- Programmable Gamma Correction Curve
- Programmable drive duty ratio: 1/16 up to 1/132 in steps of 8
- On-Chip Oscillator
- Non-Volatile Memory (OTP) for VCOM calibration
- Available in COG package with interlaced Gate Output in both sides

3 ORDERING INFORMATION

Ordering Part Number	SEG(x RGB)	COM	Package Form	Reference	Remark
SSD1283AZ	132	132	Gold Bump Die		

Table 1 - Ordering Information

4 BLOCK DIAGRAM

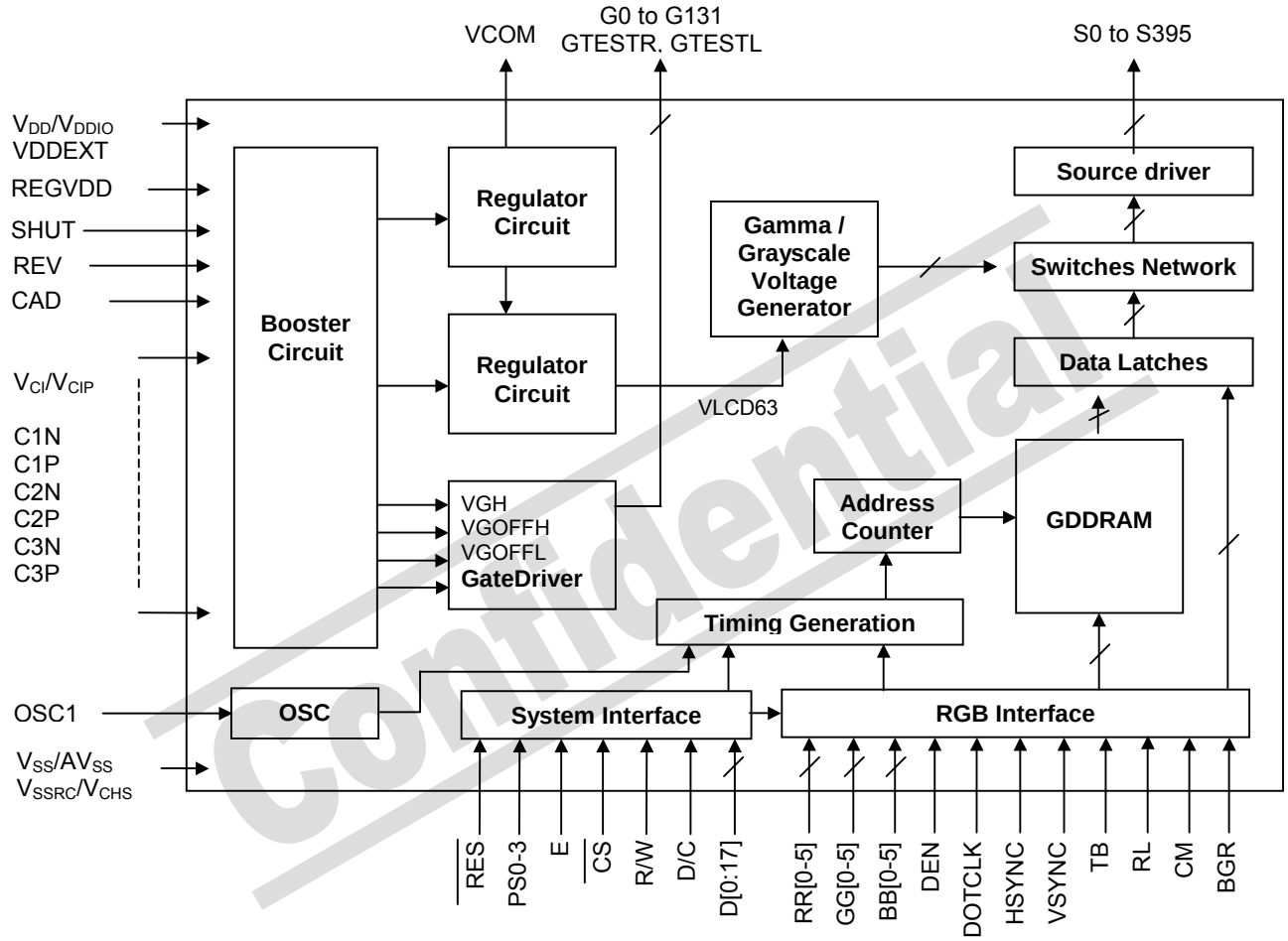
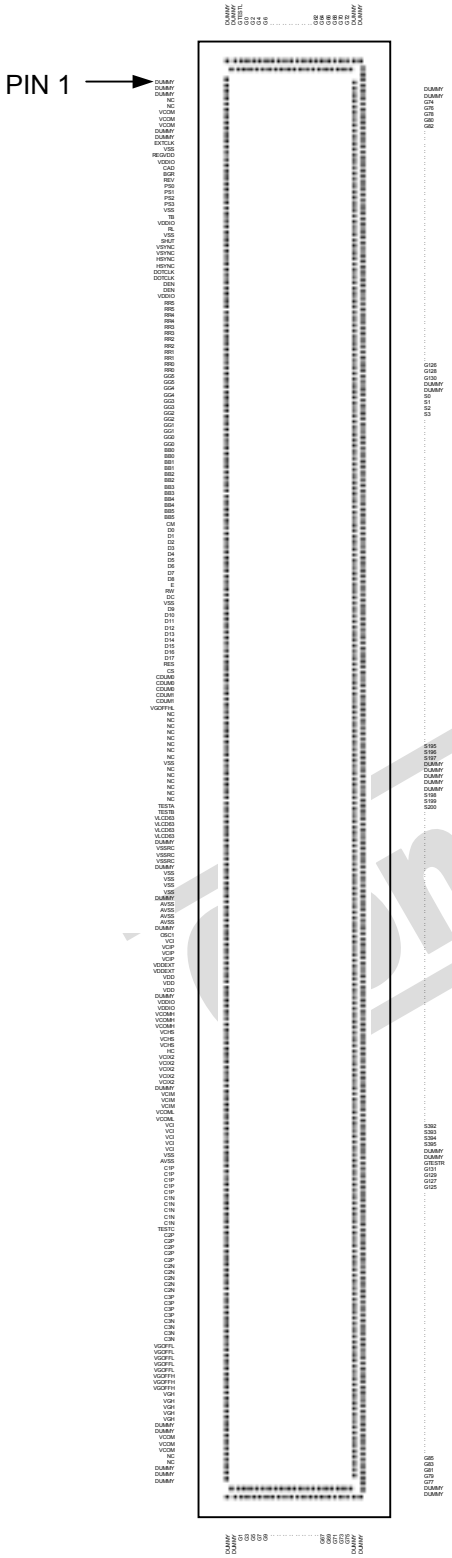
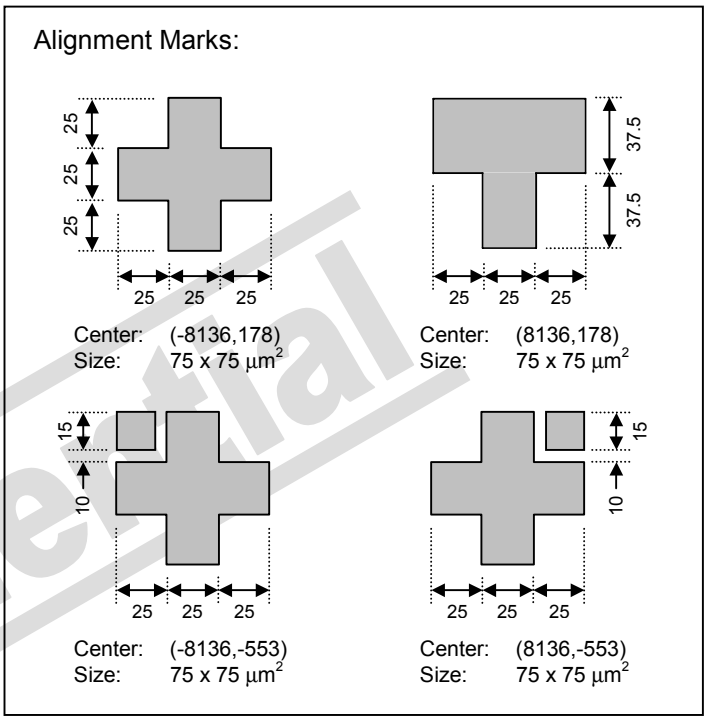


Figure 1 – SSD1283A Block Diagram

5 DIE PAD FLOOR PLAN (Gold bump face up)

Note:
1. Diagram showing the die face up.
2. Coordinates are reference to center of the chip.
3. Unit of coordinates and Size of all alignment marks are in um.
4. All alignment keys do not contain gold bump.





Die Size	18.114x1.901	mm^2
Die Thickness	406± 25	μm
Typical Bump Height	15	μm
Bump Co-planarity (within die)	<3	μm

Figure 2 – SSD1283A Die Pad Floor Plan

Table 2 – SSD1283A Series Bump Die Pad Coordinates (Bump center)

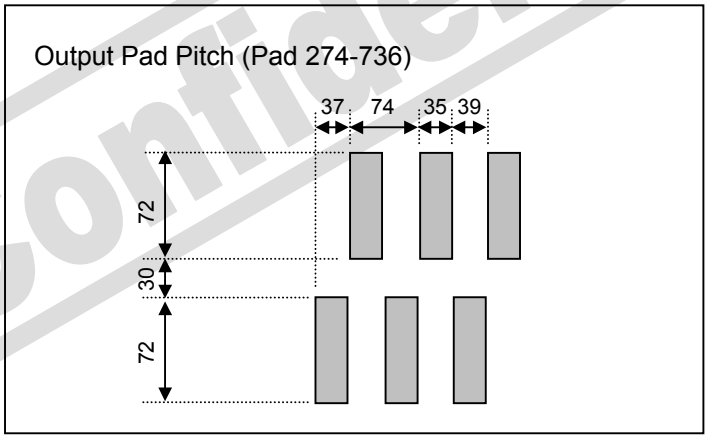
Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1	DUMMY	-8550.0	-784.0	67	BB3	-3600.0	-784.0	133	VSS	1350.0	-784.0	199	C3P	6300.0	-784.0
2	DUMMY	-8475.0	-784.0	68	BB3	-3525.0	-784.0	134	DUMMY	1425.0	-784.0	200	C3P	6375.0	-784.0
3	DUMMY	-8400.0	-784.0	69	BB4	-3450.0	-784.0	135	AVSS	1500.0	-784.0	201	C3P	6450.0	-784.0
4	NC	-8325.0	-784.0	70	BB4	-3375.0	-784.0	136	AVSS	1575.0	-784.0	202	C3P	6525.0	-784.0
5	NC	-8250.0	-784.0	71	BB5	-3300.0	-784.0	137	AVSS	1650.0	-784.0	203	C3N	6600.0	-784.0
6	VCOM	-8175.0	-784.0	72	BB5	-3225.0	-784.0	138	AVSS	1725.0	-784.0	204	C3N	6675.0	-784.0
7	VCOM	-8100.0	-784.0	73	CM	-3150.0	-784.0	139	DUMMY	1800.0	-784.0	205	C3N	6750.0	-784.0
8	VCOM	-8025.0	-784.0	74	D0	-3075.0	-784.0	140	OSC1	1875.0	-784.0	206	C3N	6825.0	-784.0
9	DUMMY	-7950.0	-784.0	75	D1	-3000.0	-784.0	141	VCI	1950.0	-784.0	207	VGOFFL	6900.0	-784.0
10	DUMMY	-7875.0	-784.0	76	D2	-2925.0	-784.0	142	VCIP	2025.0	-784.0	208	VGOFFL	6975.0	-784.0
11	EXTCLK	-7800.0	-784.0	77	D3	-2850.0	-784.0	143	VCIP	2100.0	-784.0	209	VGOFFL	7050.0	-784.0
12	VSS	-7725.0	-784.0	78	D4	-2775.0	-784.0	144	VCIP	2175.0	-784.0	210	VGOFFL	7125.0	-784.0
13	REGVDD	-7650.0	-784.0	79	D5	-2700.0	-784.0	145	VDDEXT	2250.0	-784.0	211	VGOFFL	7200.0	-784.0
14	VDDIO	-7575.0	-784.0	80	D6	-2625.0	-784.0	146	VDDEXT	2325.0	-784.0	212	VGOFFH	7275.0	-784.0
15	CAD	-7500.0	-784.0	81	D7	-2550.0	-784.0	147	VDD	2400.0	-784.0	213	VGOFFH	7350.0	-784.0
16	BGR	-7425.0	-784.0	82	D8	-2475.0	-784.0	148	VDD	2475.0	-784.0	214	VGOFFH	7425.0	-784.0
17	REV	-7350.0	-784.0	83	E($\overline{WR}$)	-2400.0	-784.0	149	VDD	2550.0	-784.0	215	VGH	7500.0	-784.0
18	PS0	-7275.0	-784.0	84	R/ $\overline{W}$ ($\overline{RD}$)	-2325.0	-784.0	150	DUMMY	2625.0	-784.0	216	VGH	7575.0	-784.0
19	PS1	-7200.0	-784.0	85	D/ $\overline{C}$	-2250.0	-784.0	151	VDDIO	2700.0	-784.0	217	VGH	7650.0	-784.0
20	PS2	-7125.0	-784.0	86	VSS	-2175.0	-784.0	152	VDDIO	2775.0	-784.0	218	VGH	7725.0	-784.0
21	PS3	-7050.0	-784.0	87	D9	-2100.0	-784.0	153	VCOMH	2850.0	-784.0	219	VGH	7800.0	-784.0
22	VSS	-6975.0	-784.0	88	D10	-2025.0	-784.0	154	VCOMH	2925.0	-784.0	220	DUMMY	7875.0	-784.0
23	TB	-6900.0	-784.0	89	D11	-1950.0	-784.0	155	VCOMH	3000.0	-784.0	221	DUMMY	7950.0	-784.0
24	VDDIO	-6825.0	-784.0	90	D12	-1875.0	-784.0	156	VCHS	3075.0	-784.0	222	VCOM	8025.0	-784.0
25	RL	-6750.0	-784.0	91	D13	-1800.0	-784.0	157	VCHS	3150.0	-784.0	223	VCOM	8100.0	-784.0
26	VSS	-6675.0	-784.0	92	D14	-1725.0	-784.0	158	VCHS	3225.0	-784.0	224	VCOM	8175.0	-784.0
27	SHUT	-6600.0	-784.0	93	D15	-1650.0	-784.0	159	HC	3300.0	-784.0	225	NC	8250.0	-784.0
28	VSYNC	-6525.0	-784.0	94	D16	-1575.0	-784.0	160	VCIX2	3375.0	-784.0	226	NC	8325.0	-784.0
29	VSYNC	-6450.0	-784.0	95	D17	-1500.0	-784.0	161	VCIX2	3450.0	-784.0	227	DUMMY	8400.0	-784.0
30	HSYNC	-6375.0	-784.0	96	$\overline{RES}$	-1425.0	-784.0	162	VCIX2	3525.0	-784.0	228	DUMMY	8475.0	-784.0
31	HSYNC	-6300.0	-784.0	97	$\overline{CS}$	-1350.0	-784.0	163	VCIX2	3600.0	-784.0	229	DUMMY	8550.0	-784.0
32	DOTCLK	-6225.0	-784.0	98	CDUM0	-1275.0	-784.0	164	VCIX2	3675.0	-784.0	230	DUMMY	8776.0	-773.5
33	DOTCLK	-6150.0	-784.0	99	CDUM0	-1200.0	-784.0	165	DUMMY	3750.0	-784.0	231	DUMMY	8674.0	-722.5
34	DEN	-6075.0	-784.0	100	CDUM0	-1125.0	-784.0	166	VCIM	3825.0	-784.0	232	G1	8776.0	-678.5
35	DEN	-6000.0	-784.0	101	CDUM1	-1050.0	-784.0	167	VCIM	3900.0	-784.0	233	G3	8674.0	-641.5
36	VDDIO	-5925.0	-784.0	102	CDUM1	-975.0	-784.0	168	VCIM	3975.0	-784.0	234	G5	8776.0	-604.5
37	RR5	-5850.0	-784.0	103	VGOFFHL	-900.0	-784.0	169	VCOML	4050.0	-784.0	235	G7	8674.0	-567.5
38	RR5	-5775.0	-784.0	104	NC	-825.0	-784.0	170	VCOML	4125.0	-784.0	236	G9	8776.0	-530.5
39	RR4	-5700.0	-784.0	105	NC	-750.0	-784.0	171	VCI	4200.0	-784.0	237	G11	8674.0	-493.5
40	RR4	-5625.0	-784.0	106	NC	-675.0	-784.0	172	VCI	4275.0	-784.0	238	G13	8776.0	-456.5
41	RR3	-5550.0	-784.0	107	NC	-600.0	-784.0	173	VCI	4350.0	-784.0	239	G15	8674.0	-419.5
42	RR3	-5475.0	-784.0	108	NC	-525.0	-784.0	174	VCI	4425.0	-784.0	240	G17	8776.0	-382.5
43	RR2	-5400.0	-784.0	109	NC	-450.0	-784.0	175	VCI	4500.0	-784.0	241	G19	8674.0	-345.5
44	RR2	-5325.0	-784.0	110	NC	-375.0	-784.0	176	VSS	4575.0	-784.0	242	G21	8776.0	-308.5
45	RR1	-5250.0	-784.0	111	NC	-300.0	-784.0	177	AVSS	4650.0	-784.0	243	G23	8674.0	-271.5
46	RR1	-5175.0	-784.0	112	VSS	-225.0	-784.0	178	C1P	4725.0	-784.0	244	G25	8776.0	-234.5
47	RR0	-5100.0	-784.0	113	NC	-150.0	-784.0	179	C1P	4800.0	-784.0	245	G27	8674.0	-197.5
48	RR0	-5025.0	-784.0	114	NC	-75.0	-784.0	180	C1P	4875.0	-784.0	246	G29	8776.0	-160.5
49	GG5	-4950.0	-784.0	115	NC	0.0	-784.0	181	C1P	4950.0	-784.0	247	G31	8674.0	-123.5
50	GG5	-4875.0	-784.0	116	NC	75.0	-784.0	182	C1P	5025.0	-784.0	248	G33	8776.0	-86.5
51	GG4	-4800.0	-784.0	117	NC	150.0	-784.0	183	C1N	5100.0	-784.0	249	G35	8674.0	-49.5
52	GG4	-4725.0	-784.0	118	NC	225.0	-784.0	184	C1N	5175.0	-784.0	250	G37	8776.0	-12.5
53	GG3	-4650.0	-784.0	119	TESTA	300.0	-784.0	185	C1N	5250.0	-784.0	251	G39	8674.0	24.5
54	GG3	-4575.0	-784.0	120	TESTB	375.0	-784.0	186	C1N	5325.0	-784.0	252	G41	8776.0	61.5
55	GG2	-4500.0	-784.0	121	VLCD63	450.0	-784.0	187	C1N	5400.0	-784.0	253	G43	8674.0	98.5
56	GG2	-4425.0	-784.0	122	VLCD63	525.0	-784.0	188	TESTC	5475.0	-784.0	254	G45	8776.0	135.5
57	GG1	-4350.0	-784.0	123	VLCD63	600.0	-784.0	189	C2P	5550.0	-784.0	255	G47	8674.0	172.5
58	GG1	-4275.0	-784.0	124	VLCD63	675.0	-784.0	190	C2P	5625.0	-784.0	256	G49	8776.0	209.5
59	GG0	-4200.0	-784.0	125	DUMMY	750.0	-784.0	191	C2P	5700.0	-784.0	257	G51	8674.0	246.5
60	GG0	-4125.0	-784.0	126	VSSRC	825.0	-784.0	192	C2P	5775.0	-784.0	258	G53	8776.0	283.5
61	BB0	-4050.0	-784.0	127	VSSRC	900.0	-784.0	193	C2P	5850.0	-784.0	259	G55	8674.0	320.5
62	BB0	-3975.0	-784.0	128	VSSRC	975.0	-784.0	194	C2N	5925.0	-784.0	260	G57	8776.0	357.5
63	BB1	-3900.0	-784.0	129	DUMMY	1050.0	-784.0	195	C2N	6000.0	-784.0	261	G59	8674.0	394.5
64	BB1	-3825.0	-784.0	130	VSS	1125.0	-784.0	196	C2N	6075.0	-784.0	262	G61	8776.0	431.5
65	BB2	-3750.0	-784.0	131	VSS	1200.0	-784.0	197	C2N	6150.0	-784.0	263	G63	8674.0	468.5
66	BB2	-3675.0	-784.0	132	VSS	1275.0	-784.0	198	C2N	6225.0	-784.0	264	G65	8776.0	505.5

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
265	G67	8674.0	542.5	331	S369	6438.0	737.5	397	S303	3996.0	737.5	463	S237	1554.0	737.5
266	G69	8776.0	579.5	332	S368	6401.0	839.5	398	S302	3959.0	839.5	464	S236	1517.0	839.5
267	G71	8674.0	616.5	333	S367	6364.0	737.5	399	S301	3922.0	737.5	465	S235	1480.0	737.5
268	G73	8776.0	653.5	334	S366	6327.0	839.5	400	S300	3885.0	839.5	466	S234	1443.0	839.5
269	G75	8674.0	690.5	335	S365	6290.0	737.5	401	S299	3848.0	737.5	467	S233	1406.0	737.5
270	DUMMY	8776.0	734.5	336	S364	6253.0	839.5	402	S298	3811.0	839.5	468	S232	1369.0	839.5
271	DUMMY	8776.0	807.5	337	S363	6216.0	737.5	403	S297	3774.0	737.5	469	S231	1332.0	737.5
272	DUMMY	8686.0	839.5	338	S362	6179.0	839.5	404	S296	3737.0	839.5	470	S230	1295.0	839.5
273	DUMMY	8613.0	839.5	339	S361	6142.0	737.5	405	S295	3700.0	737.5	471	S229	1258.0	737.5
274	G77	8547.0	839.5	340	S360	6105.0	839.5	406	S294	3663.0	839.5	472	S228	1221.0	839.5
275	G79	8510.0	737.5	341	S359	6068.0	737.5	407	S293	3626.0	737.5	473	S227	1184.0	737.5
276	G81	8473.0	839.5	342	S358	6031.0	839.5	408	S292	3589.0	839.5	474	S226	1147.0	839.5
277	G83	8436.0	737.5	343	S357	5994.0	737.5	409	S291	3552.0	737.5	475	S225	1110.0	737.5
278	G85	8399.0	839.5	344	S356	5957.0	839.5	410	S290	3515.0	839.5	476	S224	1073.0	839.5
279	G87	8362.0	737.5	345	S355	5920.0	737.5	411	S289	3478.0	737.5	477	S223	1036.0	737.5
280	G89	8325.0	839.5	346	S354	5883.0	839.5	412	S288	3441.0	839.5	478	S222	999.0	839.5
281	G91	8288.0	737.5	347	S353	5846.0	737.5	413	S287	3404.0	737.5	479	S221	962.0	737.5
282	G93	8251.0	839.5	348	S352	5809.0	839.5	414	S286	3367.0	839.5	480	S220	925.0	839.5
283	G95	8214.0	737.5	349	S351	5772.0	737.5	415	S285	3330.0	737.5	481	S219	888.0	737.5
284	G97	8177.0	839.5	350	S350	5735.0	839.5	416	S284	3293.0	839.5	482	S218	851.0	839.5
285	G99	8140.0	737.5	351	S349	5698.0	737.5	417	S283	3256.0	737.5	483	S217	814.0	737.5
286	G101	8103.0	839.5	352	S348	5661.0	839.5	418	S282	3219.0	839.5	484	S216	777.0	839.5
287	G103	8066.0	737.5	353	S347	5624.0	737.5	419	S281	3182.0	737.5	485	S215	740.0	737.5
288	G105	8029.0	839.5	354	S346	5587.0	839.5	420	S280	3145.0	839.5	486	S214	703.0	839.5
289	G107	7992.0	737.5	355	S345	5550.0	737.5	421	S279	3108.0	737.5	487	S213	666.0	737.5
290	G109	7955.0	839.5	356	S344	5513.0	839.5	422	S278	3071.0	839.5	488	S212	629.0	839.5
291	G111	7918.0	737.5	357	S343	5476.0	737.5	423	S277	3034.0	737.5	489	S211	592.0	737.5
292	G113	7881.0	839.5	358	S342	5439.0	839.5	424	S276	2997.0	839.5	490	S210	555.0	839.5
293	G115	7844.0	737.5	359	S341	5402.0	737.5	425	S275	2960.0	737.5	491	S209	518.0	737.5
294	G117	7807.0	839.5	360	S340	5365.0	839.5	426	S274	2923.0	839.5	492	S208	481.0	839.5
295	G119	7770.0	737.5	361	S339	5328.0	737.5	427	S273	2886.0	737.5	493	S207	444.0	737.5
296	G121	7733.0	839.5	362	S338	5291.0	839.5	428	S272	2849.0	839.5	494	S206	407.0	839.5
297	G123	7696.0	737.5	363	S337	5254.0	737.5	429	S271	2812.0	737.5	495	S205	370.0	737.5
298	G125	7659.0	839.5	364	S336	5217.0	839.5	430	S270	2775.0	839.5	496	S204	333.0	839.5
299	G127	7622.0	737.5	365	S335	5180.0	737.5	431	S269	2738.0	737.5	497	S203	296.0	737.5
300	G129	7585.0	839.5	366	S334	5143.0	839.5	432	S268	2701.0	839.5	498	S202	259.0	839.5
301	G131	7548.0	737.5	367	S333	5106.0	737.5	433	S267	2664.0	737.5	499	S201	222.0	737.5
302	GTESTR	7511.0	839.5	368	S332	5069.0	839.5	434	S266	2627.0	839.5	500	S200	185.0	839.5
303	DUMMY	7474.0	737.5	369	S331	5032.0	737.5	435	S265	2590.0	737.5	501	S199	148.0	737.5
304	DUMMY	7437.0	839.5	370	S330	4995.0	839.5	436	S264	2553.0	839.5	502	S198	111.0	839.5
305	S395	7400.0	737.5	371	S329	4958.0	737.5	437	S263	2516.0	737.5	503	DUMMY	74.0	737.5
306	S394	7363.0	839.5	372	S328	4921.0	839.5	438	S262	2479.0	839.5	504	DUMMY	37.0	839.5
307	S393	7326.0	737.5	373	S327	4884.0	737.5	439	S261	2442.0	737.5	505	DUMMY	0.0	737.5
308	S392	7289.0	839.5	374	S326	4847.0	839.5	440	S260	2405.0	839.5	506	DUMMY	-37.0	839.5
309	S391	7252.0	737.5	375	S325	4810.0	737.5	441	S259	2368.0	737.5	507	DUMMY	-74.0	737.5
310	S390	7215.0	839.5	376	S324	4773.0	839.5	442	S258	2331.0	839.5	508	S197	-111.0	839.5
311	S389	7178.0	737.5	377	S323	4736.0	737.5	443	S257	2294.0	737.5	509	S196	-148.0	737.5
312	S388	7141.0	839.5	378	S322	4699.0	839.5	444	S256	2257.0	839.5	510	S195	-185.0	839.5
313	S387	7104.0	737.5	379	S321	4662.0	737.5	445	S255	2220.0	737.5	511	S194	-222.0	737.5
314	S386	7067.0	839.5	380	S320	4625.0	839.5	446	S254	2183.0	839.5	512	S193	-259.0	839.5
315	S385	7030.0	737.5	381	S319	4588.0	737.5	447	S253	2146.0	737.5	513	S192	-296.0	737.5
316	S384	6993.0	839.5	382	S318	4551.0	839.5	448	S252	2109.0	839.5	514	S191	-333.0	839.5
317	S383	6956.0	737.5	383	S317	4514.0	737.5	449	S251	2072.0	737.5	515	S190	-370.0	737.5
318	S382	6919.0	839.5	384	S316	4477.0	839.5	450	S250	2035.0	839.5	516	S189	-407.0	839.5
319	S381	6882.0	737.5	385	S315	4440.0	737.5	451	S249	1998.0	737.5	517	S188	-444.0	737.5
320	S380	6845.0	839.5	386	S314	4403.0	839.5	452	S248	1961.0	839.5	518	S187	-481.0	839.5
321	S379	6808.0	737.5	387	S313	4366.0	737.5	453	S247	1924.0	737.5	519	S186	-518.0	737.5
322	S378	6771.0	839.5	388	S312	4329.0	839.5	454	S246	1887.0	839.5	520	S185	-555.0	839.5
323	S377	6734.0	737.5	389	S311	4292.0	737.5	455	S245	1850.0	737.5	521	S184	-592.0	737.5
324	S376	6697.0	839.5	390	S310	4255.0	839.5	456	S244	1813.0	839.5	522	S183	-629.0	839.5
325	S375	6660.0	737.5	391	S309	4218.0	737.5	457	S243	1776.0	737.5	523	S182	-666.0	737.5
326	S374	6623.0	839.5	392	S308	4181.0	839.5	458	S242	1739.0	839.5	524	S181	-703.0	839.5
327	S373	6586.0	737.5	393	S307	4144.0	737.5	459	S241	1702.0	737.5	525	S180	-740.0	737.5
328	S372	6549.0	839.5	394	S306	4107.0	839.5	460	S240	1665.0	839.5	526	S179	-777.0	839.5
329	S371	6512.0	737.5	395	S305	4070.0	737.5	461	S239	1628.0	737.5	527	S178	-814.0	737.5
330	S370	6475.0	839.5	396	S304	4033.0	839.5	462	S238	1591.0	839.5	528	S177	-851.0	839.5

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
529	S176	-888.0	737.5	595	S110	-3330.0	737.5	661	S44	-5772.0	737.5	727	G92	-8214.0	737.5
530	S175	-925.0	839.5	596	S109	-3367.0	839.5	662	S43	-5809.0	839.5	728	G90	-8251.0	839.5
531	S174	-962.0	737.5	597	S108	-3404.0	737.5	663	S42	-5846.0	737.5	729	G88	-8288.0	737.5
532	S173	-999.0	839.5	598	S107	-3441.0	839.5	664	S41	-5883.0	839.5	730	G86	-8325.0	839.5
533	S172	-1036.0	737.5	599	S106	-3478.0	737.5	665	S40	-5920.0	737.5	731	G84	-8362.0	737.5
534	S171	-1073.0	839.5	600	S105	-3515.0	839.5	666	S39	-5957.0	839.5	732	G82	-8399.0	839.5
535	S170	-1110.0	737.5	601	S104	-3552.0	737.5	667	S38	-5994.0	737.5	733	G80	-8436.0	737.5
536	S169	-1147.0	839.5	602	S103	-3589.0	839.5	668	S37	-6031.0	839.5	734	G78	-8473.0	839.5
537	S168	-1184.0	737.5	603	S102	-3626.0	737.5	669	S36	-6068.0	737.5	735	G76	-8510.0	737.5
538	S167	-1221.0	839.5	604	S101	-3663.0	839.5	670	S35	-6105.0	839.5	736	G74	-8547.0	839.5
539	S166	-1258.0	737.5	605	S100	-3700.0	737.5	671	S34	-6142.0	737.5	737	DUMMY	-8613.0	839.5
540	S165	-1295.0	839.5	606	S99	-3737.0	839.5	672	S33	-6179.0	839.5	738	DUMMY	-8686.0	839.5
541	S164	-1332.0	737.5	607	S98	-3774.0	737.5	673	S32	-6216.0	737.5	739	DUMMY	-8776.0	807.5
542	S163	-1369.0	839.5	608	S97	-3811.0	839.5	674	S31	-6253.0	839.5	740	DUMMY	-8776.0	734.5
543	S162	-1406.0	737.5	609	S96	-3848.0	737.5	675	S30	-6290.0	737.5	741	G72	-8674.0	690.5
544	S161	-1443.0	839.5	610	S95	-3885.0	839.5	676	S29	-6327.0	839.5	742	G70	-8776.0	653.5
545	S160	-1480.0	737.5	611	S94	-3922.0	737.5	677	S28	-6364.0	737.5	743	G68	-8674.0	616.5
546	S159	-1517.0	839.5	612	S93	-3959.0	839.5	678	S27	-6401.0	839.5	744	G66	-8776.0	579.5
547	S158	-1554.0	737.5	613	S92	-3996.0	737.5	679	S26	-6438.0	737.5	745	G64	-8674.0	542.5
548	S157	-1591.0	839.5	614	S91	-4033.0	839.5	680	S25	-6475.0	839.5	746	G62	-8776.0	505.5
549	S156	-1628.0	737.5	615	S90	-4070.0	737.5	681	S24	-6512.0	737.5	747	G60	-8674.0	468.5
550	S155	-1665.0	839.5	616	S89	-4107.0	839.5	682	S23	-6549.0	839.5	748	G58	-8776.0	431.5
551	S154	-1702.0	737.5	617	S88	-4144.0	737.5	683	S22	-6586.0	737.5	749	G56	-8674.0	394.5
552	S153	-1739.0	839.5	618	S87	-4181.0	839.5	684	S21	-6623.0	839.5	750	G54	-8776.0	357.5
553	S152	-1776.0	737.5	619	S86	-4218.0	737.5	685	S20	-6660.0	737.5	751	G52	-8674.0	320.5
554	S151	-1813.0	839.5	620	S85	-4255.0	839.5	686	S19	-6697.0	839.5	752	G50	-8776.0	283.5
555	S150	-1850.0	737.5	621	S84	-4292.0	737.5	687	S18	-6734.0	737.5	753	G48	-8674.0	246.5
556	S149	-1887.0	839.5	622	S83	-4329.0	839.5	688	S17	-6771.0	839.5	754	G46	-8776.0	209.5
557	S148	-1924.0	737.5	623	S82	-4366.0	737.5	689	S16	-6808.0	737.5	755	G44	-8674.0	172.5
558	S147	-1961.0	839.5	624	S81	-4403.0	839.5	690	S15	-6845.0	839.5	756	G42	-8776.0	135.5
559	S146	-1998.0	737.5	625	S80	-4440.0	737.5	691	S14	-6882.0	737.5	757	G40	-8674.0	98.5
560	S145	-2035.0	839.5	626	S79	-4477.0	839.5	692	S13	-6919.0	839.5	758	G38	-8776.0	61.5
561	S144	-2072.0	737.5	627	S78	-4514.0	737.5	693	S12	-6956.0	737.5	759	G36	-8674.0	24.5
562	S143	-2109.0	839.5	628	S77	-4551.0	839.5	694	S11	-6993.0	839.5	760	G34	-8776.0	-12.5
563	S142	-2146.0	737.5	629	S76	-4588.0	737.5	695	S10	-7030.0	737.5	761	G32	-8674.0	-49.5
564	S141	-2183.0	839.5	630	S75	-4625.0	839.5	696	S9	-7067.0	839.5	762	G30	-8776.0	-86.5
565	S140	-2220.0	737.5	631	S74	-4662.0	737.5	697	S8	-7104.0	737.5	763	G28	-8674.0	-123.5
566	S139	-2257.0	839.5	632	S73	-4699.0	839.5	698	S7	-7141.0	839.5	764	G26	-8776.0	-160.5
567	S138	-2294.0	737.5	633	S72	-4736.0	737.5	699	S6	-7178.0	737.5	765	G24	-8674.0	-197.5
568	S137	-2331.0	839.5	634	S71	-4773.0	839.5	700	S5	-7215.0	839.5	766	G22	-8776.0	-234.5
569	S136	-2368.0	737.5	635	S70	-4810.0	737.5	701	S4	-7252.0	737.5	767	G20	-8674.0	-271.5
570	S135	-2405.0	839.5	636	S69	-4847.0	839.5	702	S3	-7289.0	839.5	768	G18	-8776.0	-308.5
571	S134	-2442.0	737.5	637	S68	-4884.0	737.5	703	S2	-7326.0	737.5	769	G16	-8674.0	-345.5
572	S133	-2479.0	839.5	638	S67	-4921.0	839.5	704	S1	-7363.0	839.5	770	G14	-8776.0	-382.5
573	S132	-2516.0	737.5	639	S66	-4958.0	737.5	705	S0	-7400.0	737.5	771	G12	-8674.0	-419.5
574	S131	-2553.0	839.5	640	S65	-4995.0	839.5	706	DUMMY	-7437.0	839.5	772	G10	-8776.0	-456.5
575	S130	-2590.0	737.5	641	S64	-5032.0	737.5	707	DUMMY	-7474.0	737.5	773	G8	-8674.0	-493.5
576	S129	-2627.0	839.5	642	S63	-5069.0	839.5	708	G130	-7511.0	839.5	774	G6	-8776.0	-530.5
577	S128	-2664.0	737.5	643	S62	-5106.0	737.5	709	G128	-7548.0	737.5	775	G4	-8674.0	-567.5
578	S127	-2701.0	839.5	644	S61	-5143.0	839.5	710	G126	-7585.0	839.5	776	G2	-8776.0	-604.5
579	S126	-2738.0	737.5	645	S60	-5180.0	737.5	711	G124	-7622.0	737.5	777	G0	-8674.0	-641.5
580	S125	-2775.0	839.5	646	S59	-5217.0	839.5	712	G122	-7659.0	839.5	778	GTESTL	-8776.0	-678.5
581	S124	-2812.0	737.5	647	S58	-5254.0	737.5	713	G120	-7696.0	737.5	779	DUMMY	-8674.0	-722.5
582	S123	-2849.0	839.5	648	S57	-5291.0	839.5	714	G118	-7733.0	839.5	780	DUMMY	-8776.0	-773.5
583	S122	-2886.0	737.5	649	S56	-5328.0	737.5	715	G116	-7770.0	737.5				
584	S121	-2923.0	839.5	650	S55	-5365.0	839.5	716	G114	-7807.0	839.5				
585	S120	-2960.0	737.5	651	S54	-5402.0	737.5	717	G112	-7844.0	737.5				
586	S119	-2997.0	839.5	652	S53	-5439.0	839.5	718	G110	-7881.0	839.5				
587	S118	-3034.0	737.5	653	S52	-5476.0	737.5	719	G108	-7918.0	737.5				
588	S117	-3071.0	839.5	654	S51	-5513.0	839.5	720	G106	-7955.0	839.5				
589	S116	-3108.0	737.5	655	S50	-5550.0	737.5	721	G104	-7992.0	737.5				
590	S115	-3145.0	839.5	656	S49	-5587.0	839.5	722	G102	-8029.0	839.5				
591	S114	-3182.0	737.5	657	S48	-5624.0	737.5	723	G100	-8066.0	737.5				
592	S113	-3219.0	839.5	658	S47	-5661.0	839.5	724	G98	-8103.0	839.5				
593	S112	-3256.0	737.5	659	S46	-5698.0	737.5	725	G96	-8140.0	737.5				
594	S111	-3293.0	839.5	660	S45	-5735.0	839.5	726	G94	-8177.0	839.5				

Bump Size

PAD#	X [um]	Y [um]	Pad pitch [um] (Min)
Pad 1-229	51	93	37
Pad 232-269, 741-778	72	35	37
Pad 274-736	35	72	37
Pad 272-3, 737-8	49	72	37
Pad 230-231, 270-271, 739-740, 779-780	72	49	37



6 PIN DESCRIPTION

Table 3 – SSD1283A pin description

Name	Type	Function	Function
CM	I	Logic Control	Input pin to select 262k-color or 8-color display mode. After entered 8-color mode, the driving method will be frame inversion mode, and only MSB of the data Red, Green and Blue will be considered. o Connect to V_{DDIO} for 262k-color display mode o Connect to V_{SS} for 8-color display mode
RR[5:0]	I	Graphic Display Data	Graphic Data Input Pins: Red Data – 6-bits Green Data – 6-bits Blue Data – 6-bits
GG[5:0]			
BB[5:0]			
DEN	I	Display Timing Signals	Display enable pin from controller.
VSYNC			Frame synchronization signal - Connect to V_{DDIO} or V_{SS} if not used
HSYNC			Line synchronization signal. - Connect to V_{DDIO} or V_{SS} if not used
DOTCLK			Dot-clock signal and oscillator source. External clock must be provided to that pin even at front or black porch non-display period - Connect to V_{DDIO} or V_{SS} if not used
SHUT	I	Logic Control	Display shut down pin in generic display mode. The driver will be put into sleep mode when SHUT = V_{DDIO} while Dmode[1:0] = 01h in register R03h - Connect to V_{DDIO} if not used
RL	I	Panel Mapping Control	Source driver data shift direction. - Connect to V_{DDIO} for display first RGB data at S0~S2 - Connect to V_{SS} for display first RGB data at S395~S393
TB			Gate driver scan direction. - Connect to V_{DDIO} for gate scan from G0 to G131 - Connect to V_{SS} for gate scan from G131 to G0
BGR			Color mapping selection pin. Refer to S0-S395 pin description - Connect to V_{DDIO} for Blue-Green-Red mapping - Connect to V_{SS} for Red-Green-Blue mapping
REV			Display reverse selection pin - Connect to V_{DDIO} for mapping data “0” to maximum pixel voltage - Connect to V_{SS} for mapping data “0” to minimum pixel voltage
CAD			Panel structure selection pin. - Connect to V_{DDIO} if Cs on gate structure is used - Connect to V_{SS} if Cs on common structure is used
PS0	I	Interface Selection	PS[3:0] = 0000 : 3-wires MCU Serial interface 0001 : 4-wires MCU Serial interface 0100 : 16 bits 68 parallel interface 0101 : 8 bits 68 parallel interface 0110 : 16 bits 80 parallel interface 0111 : 8 bits 80 parallel interface 1000 : 18 bits 68 parallel interface 1001 : 9 bits 68 parallel interface 1010 : 18 bits 80 parallel interface 1011 : 9 bits 80 parallel interface
PS1			
PS2			
PS3			
D/$\overline{C}$	I	Logic Control	Data or command
E; $\overline{RD}$			68-system : E (enable signal) 80-system : $\overline{RD}$ (read strobe signal) Serial mode : Not used and should be connected to V_{DDIO} or V_{ss}
R/$\overline{W}$; $\overline{WR}$			68-system : R/$\overline{W}$ (indicates read cycle when High, write cycle when Low) 80-system : $\overline{WR}$ (write strobe signal) Serial mode : Not used and should be connected to V_{DDIO} or V_{ss}
D0-D14	I/O	Data Bus	For parallel mode, 8/9/16/18 bit interface, refer to Section Interface Mapping for definition. For serial mode, D15-D17 are used. Unused pins should be connected to Vss
D15 (SDO)	I/O		
D16 (SCK)	I		
D17 (SDI)	I		
REGVDD	I	Logic Control	Enable internal voltage regulation. - Connect to V_{DDIO} if the supply voltage for V_{DDIO} is above 2.5V - Connect to V_{SS} if the supply voltage for V_{DDIO} is below 2.5V
$\overline{RES}$	I	System Reset	System reset pin. Initialization occurs once this pin is pulled low, the minimum pulse length is 10us. A low pulse must be applied after power-on. Connect this pin to VDDIO when not used.

Name	Type	Function	Function
$\overline{CS}$	I	Logic Control	Chip select pin.
V_{DD}	Power	Power for core logic	Voltage input pin for internal logic. - If System V_{DD} > 2.5V: Connect V_{DD} to a 1uF capacitor Connect System V_{DD} to V_{DDEXT} and V_{DDIO} - If 1.65V ≤ System V_{DD} < 2.5V : Connect System V_{DD} to V_{DDEXT}, V_{DDIO} and V_{DD} - If 1.16V ≤ System V_{DD} < 1.65V : Connect V_{DD} and V_{DDEXT} to a power supply between 1.65V to 2.5V.
V_{DDEXT}	Power	Power for internal VDD regulator	
V_{DDIO}	Power	Power for interface logic pins	Connect to system VDD.
V_{SS}	Power	Ground of Power Supply	System ground pin for the IC - Connect to system ground
AV_{SS}			Ground for analog circuit - Connect to system ground
V_{SSRC}			Ground for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages. - Connect to system ground
V_{CHS}			Ground for booster circuits - Connect to system ground
V_{CI}	Power	Power supply for analog circuits	Booster input voltage pin - Connect to stable voltage source between 2.5 to 3.6V - Connect a capacitor to VSS for stabilization
V_{CIP}			Voltage supply pin for analog circuit. This pin requires a noise free path for providing accurate LCD driving voltages - Connect to VCI
V_{CIX2}	O	Booster Output	Equals to 2 x V_{CI} - Connect a capacitor for stabilization
V_{CIM}	O	Booster Output	Negative voltage of V_{CI} - Connect a capacitor for stabilization.
V_{COMH}	O	Voltages for VCOM Signal	This pin indicates a high level of Vcom generated in driving the Vcom alternation. - Leave this pin open.
V_{COML}			This pin indicates a low level of Vcom generated in driving the Vcom alternation. - Leave this pin open.
V_{LCD63}	O	LCD Driving Voltages	This pin is the maximum source driver voltage. - Leave this pin open.
V_{GH}			A positive power output pin for gate driver. - Connect a capacitor for stabilization
V_{GOFFL}			A negative power output pin for gate driver. - Connect a capacitor for stabilization
V_{GOFFH}			When Cs on gate structure is used, this pin indicates a high level of Vgoff. - Connect a capacitor for stabilization. When Cs on Com structure is used - Leave this pin open.
V_{GOFFHL}			When Cs on gate structure is used, this pin indicates minimum power output for Vgoffh. - Charge recycling. Connect a capacitor to VCOM When Cs on Com structure is used - Leave this pin open.
C1N	I	Booster pins	- Connect a capacitor to C1P
C2N			- Connect a capacitor to C2P
C3N			- Connect a capacitor to C3P
C1P			- Connect a capacitor to C1N
C2P			- Connect a capacitor to C2N
C3P			- Connect a capacitor to C3N
CDUM0	I	Analog	Charge recycling. Connect a capacitor to VSS
CDUM1	I	Analog	Charge recycling. Connect a capacitor to VSS
TESTA	I	IC Testing Signal	Test pin of the internal circuit. Leave connection open. Optional to insert test point in FPC for development evaluation.
TESTB	I	OSC input	An internal oscillator reference pin, connect a resistor to VCI. Float this pin when using the internal oscillator.
TESTC			
OSC1			
EXTCLK	I	LCD Driving Signals	A clock input pin for internal oscillator. Connect to VSS when using the internal oscillator.
VCOM	O		A power supply for the TFT-display common electrode.
HC	I	Booster pins	Booster mode select pin -Connect to VCIM if use VCIX3 mode -Connect to VCHS if use VCIX2 mode

Name	Type	Function	Function
GTESTR, GTESTL			Gate driver output test pins. Leave it disconnected when using Cs on Common structure
G0-G131			Gate driver output pins. This pin output either VGH, VgoffH or VgoffL level.
S0-S395			Source driver output pins. S(3n) : display Red if BGR = Low, Blue if BGR = High. S(3n+1) : display Green. S(3n+2) : display Blue if BGR = Low, Red if BGR = High.
NC			These pins must be left open and cannot be connected
DUMMY			Pins that are not connected inside the IC and floated. They can be connected to any voltage or shorted together.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 System Interface

The System Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS3, PS2, PS1 and PS0 pins. Please refer to Section Die Pin Assignment .

a) MPU Parallel 6800-series Interface

The parallel Interface consists of 18 bi-directional data pins (D_{17} – D_0), R/$\overline{W}$, D/$\overline{C}$, E and $\overline{CS}$. R/$\overline{W}$ input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. R/$\overline{W}$ input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E input serves as data latch signal (clock) when high provided that $\overline{CS}$ is low. Please refer to Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

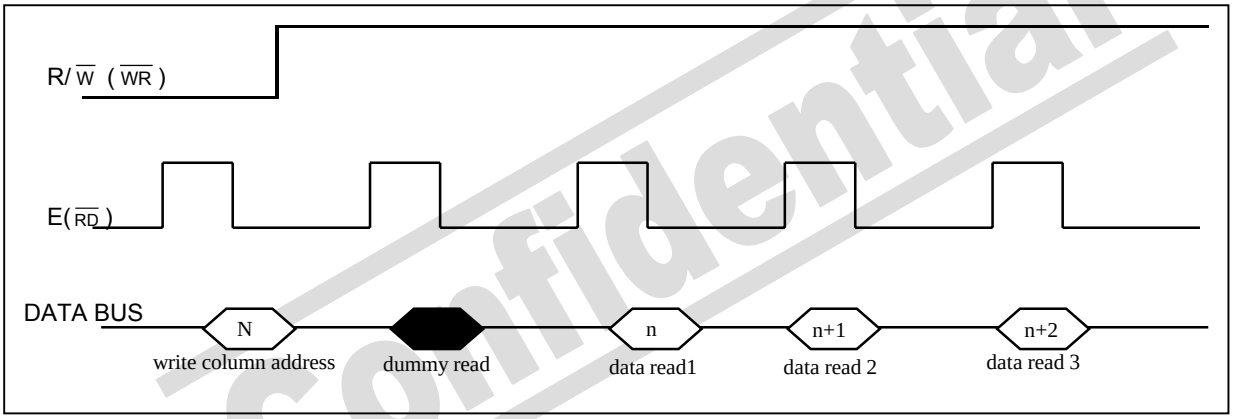


Figure 3 - Read Display Data

b) MPU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins D_{17} – D_0, $\overline{RD}$, $\overline{WR}$, D/$\overline{C}$ and $\overline{CS}$. $\overline{RD}$ input serves as data read latch signal (clock) when low provided that $\overline{CS}$ is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by D/$\overline{C}$. $\overline{WR}$ input serves as data write latch signal (clock) when low provided that $\overline{CS}$ is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by D/$\overline{C}$. A dummy read is also required before the first actual display data read for 8080-series interface.

c) MPU 4-lines Serial Peripheral Interface

The 4-lines serial peripheral Interface consists of serial clock SCK, serial data SDA, D/$\overline{C}$ and $\overline{CS}$. SDA is shifted into 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6 …… data bit 0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock.

d) MPU 3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while D/$\overline{C}$ is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/$\overline{C}$ bit, D7 to D0 bit. The D/$\overline{C}$ bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/$\overline{C}$ bit = 1) or the command register (D/$\overline{C}$ bit = 0).

	6800 – series Parallel Interface	**8080 – series Parallel Interface**	**MCU Serial Interface**
Data Read	18/16/9/8-bits	18/16/9/8-bits	No
Data Write	18/16/9/8-bits	18/16/9/8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	8-bits

Table 4 - Data bus selection modes

7.2 Address Counter (AC)

The address counter (AC) assigns address to the GDDRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.
After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

7.3 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 RGB x 132 x 18 / 8 = 39,204 bytes. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command “Data Output/Scan direction” for detail description.
Four pages of display data forms a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command “Set area Scroll” and “Set Scroll Start”.

7.4 Gamma/Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma-adjusting resistor. 262,144 possible colors can be displayed when 1 byte = 18 bit. For details, see the gamma-adjusting resistor.

7.5 Booster and Regulator Circuit

These two functional blocks generate the voltage of VGH, VGOFFL, VCOM levels and Vlcd0~63 which are necessary for operating a TFT LCD.

7.6 Oscillation Circuit (OSC)

This module is an On-Chip low power RC oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

7.7 Data Latches

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

8 COMMAND TABLE

Table 5 - Command Table

R/W	D/C	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	*	*	*	*	*	*	*	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	**R**	Index
1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	**SR**	Status Read
0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSCEN	**R00h**	Oscillation Start
1	1	0	0	0	1	0	0	1	0	1	0	0	0	0	0	1	1		Device code read
0	1	0	0	REV	CAD	BGR	SM	TB	RL	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0	**R01h**	Driver output control
0	1	0	0	0	0	FLD	0	B/C	EOR	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0	**R02h**	LCD drive AC control
0	1	VS Mode	DFM1	DFM0	TRANS	OEDef	WMode	DMode1	DMode0	TY1	TY2	ID/1	ID/0	AM	LG2	LG1	LG0	**R03h**	Entry mode
0	1	CPR5	CPR4	CPR3	CPR2	CPR1	CPR0	0	0	CPG5	CPG4	CPG3	CPG2	CPG1	CPG0	0	0	**R04h**	Compare register (1)
0	1	0	0	0	0	0	0	0	0	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0	0	0	**R05h**	Compare register (2)
0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0	**R07h**	Display control
																		R08h	Reserved
																		R09h	Reserved
0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0	**R0Bh**	Frame cycle control
																		R0Ch	Reserved
																		R0Dh	Reserved
																		R0Eh	Reserved
0	1	DOT	DCY2	DCY1	DCY0	BTH2	BTH1	BTH0	1	1	1	DC1	DC0	AP2	AP1	AP0	SLP	**R10h**	Power control (1)
0	1	0	0	0	0	0	0	0	0	0	0	0	PU1	PU0	1	0	0	**R11h**	Power control (2)
0	1	0	0	0	0	0	1	1	SX263B	V63SH	0	0	0	VRH3	VRH2	VRH1	VRH0	**R12h**	Power control (3)
0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0	**R13h**	Power control (4)
																		R15h	Reserved
0	1	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	**R16h**	Horizontal Porch
0	1	0	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	**R17h**	Vertical Porch
																		R1Ch	Reserved
																		R1Dh	Reserved
0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	**R1Eh**	Power control (5)
0	1	0	0	0	0	0	0	0	0	0	0	VCMR5	VCMR4	VCMR3	VCMR2	VCMR1	VCMR0	**R1Fh**	Power control (6)
0	1	AD[15:0]																	
0	1	Data[17:0] mapping depends on the interface setting																	
1	1																		
0	1	WMR5	WMR4	WMR3	WMR2	WMR1	WMR0	0	0	WMG5	WMG4	WMG3	WMG2	WMG1	WMG0	0	0	**R23h**	RAM write data mask (1)
0	1	0	0	0	0	0	0	0	0	WMB5	WMB4	WMB3	WMB2	WMB1	WMB0	0	0	**R24h**	RAM write data mask (2)
0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	**R28h**	VCOM OTP (1)
0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	**R29h**	VCOM OTP (2)
R/W	**D/C**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**

0	1																	**R2A-2Fh**	Test Commands
0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00	**R30h**	γ control (1)
0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20	**R31h**	γ control (2)
0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40	**R32h**	γ control (3)
0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00	**R33h**	γ control (4)
0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00	**R34h**	γ control (5)
0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20	**R35h**	γ control (6)
0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40	**R36h**	γ control (7)
0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00	**R37h**	γ control (8)
0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00	**R38h**	γ control (9)
0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00	**R39h**	γ control (10)
0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	**R40h**	Gate scan starting position
0	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10	**R41h**	Vertical scroll control
0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	**R42h**	First display drive position
0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	**R43h**	Second display drive position
0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	**R44h**	Horizontal RAM address position
0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	**R45h**	Vertical RAM address position
Extended Command Registers																			
0	1	0	0	0	0	0	1	0	1	0	1	IU2	IU1	IU0	0	0	0	**R27h**	Further Bias
0	1	OSCR3	OSCR2	OSCR1	OSCR0	0	0	0	0	0	0	0	0	0	0	0	0	**R2Ch**	Oscillator frequency

Note 1 : * means don't care
Note 2 : Register bits REV, CAD, BGR, TB, RL, CM will override the corresponding hardware pins settings.

9 COMMAND DESCRIPTIONS

Index / Status / Display control Instruction

Index (IR)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index instruction specifies the RAM control indexes (R00h to RFFh). It sets the register number in the range of 00000000 to 11111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

Device Code Read (R00h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0	0	1	0	0	1	0	1	0	0	0	0	0	1	1

If this register is read forcibly, 1283h is read.

Oscillator (R00h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN

OSCEN: The oscillator will be turned on when OSCEN = 1, off when OSCEN = 0.

Driver Output Control (R01h) (POR = 0383h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	REV	CAD	BGR	SM	TB	RL	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0

REV: Displays all character and graphics display sections with reversal when REV = “1”. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.
Note: Register bit REV will override the REV hardware pin setting.

REV	RGB data	Source Output level	
		VCOM = ”L”	VCOM = ”H”
0	000000B	V63	V0
	000001B	V62	V1
	:	:	:
	111110B	V1	V62
	111111B	V0	V63
1	000000B	V0	V63
	000001B	V1	V62
	:	:	:
	111110B	V62	V1
	111111B	V63	V0

CAD: Set up based on retention capacitor configuration of the TFT panel.
Note: Register bit CAD will override the CAD hardware pin setting.

CAD	Retention capacitor configuration
0	Cs on Common (POR)
1	Cs on Gate

BGR: Selects the <R><G><B> arrangement. When BGR = “0” <R><G><B> color is assigned from S0. When BGR = “1” <B><G><R> color is assigned from S0.
Note: Register bit BGR will override the BGR hardware pin setting.

SM: Change scanning order of gate driver. Select the order according to the mounting method.

TB: Selects the output shift direction of the gate driver. When TB = 1, G0 shifts to G131. When TB = 0, G131 shifts to G0.
Note: Register bit TB will override the TB hardware pin setting.

RL: Selects the output shift direction of the source driver. When RL = “1”, S0 shifts to S395 and <R><G><B> color is assigned from S0. When RL = “0”, S395 shifts to S0 and <R><G><B> color is assigned from S395. Set RL bit and BGR bit when changing the dot order of R, G and B. RL setting will be ignored when display with RAM (Dmode[1:0] = 00).
Note: Register bit RL will override the RL hardware pin setting.

MUX[7:0]: Specify number of lines for the LCD driver. Setting exceeds 132 lines (MUX[7:0] = 131) will be treated as dummy line of vertical front porch. Refer to “Vertical Porch” (VBH[7:0]) setting for details.

LCD-Driving-Waveform Control (R02h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD	0	B/C	EOR	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0

FLD: Set display in interlace drive mode to protect from flicker. It splits one frame into 3 fields and drive.

B/C: When B/C = 0, frame inversion of the LCD driving signal is enabled. When B/C = 1, a N-line inversion waveform is generated and alternates in each N lines specified by bits EOR and NW[6:0].

EOR: When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines.

NW[6:0]: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). NW[6:0] alternate for every set value + 1 lines.

Entry Mode (R03h) (POR = 6830h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VSMode	DFM1	DFM0	TRANS	OEDef	WMode	DMode1	DMode0	TY1	TY0	ID1	ID0	AM	LG2	LG1	LG0

VSMode: When VSMode = 1 at Dmode[1:0] = “00”, the frame frequency will be dependent on VSYNC.

DFM[1:0]: Set the color display mode.

DFM1	DFM0	Color mode
1	1	65k color (POR)
1	0	262k color

TRANS: When TRANS = 1 and Dmode[1:0] = “1x”, transparent display is allowed.

OEDef: When OEDef = 1, OE defines the display window.
When OEDef = 0 and Dmode[1:0] = “1x”, use command R1Ch and R1Dh to define the display window

WMode: When WMode = 0, write ram from normal data bus.
When WMode = 1, write ram from generic interface.

Dmode[1:0]: SSD1283A allows data display from ram data or from generic input data. When Dmode[1:0] = “00”, it displays the ram content. When Dmode[1:0] = “01”, it displays from generic input data.

Dmode1	Dmode0	Display
0	0	Ram (POR)
0	1	Generic input
1	0	Reserved
1	1	Reserved

TY[1:0]: In 262k color mode, 16 bit parallel interface, there are three types of methods in writing data into the ram, Type A, B and C are described as below.

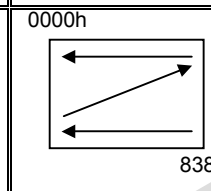
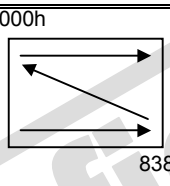
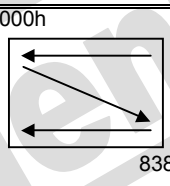
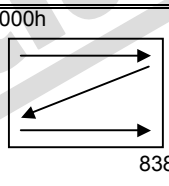
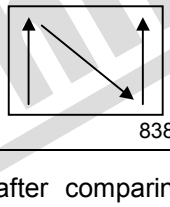
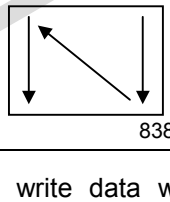
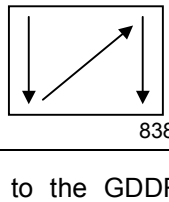
TY1	TY0	Writing mode
0	0	Type A
0	1	Type B
1	0	Type C

			Hardware pins																	
Interface	**Color mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
16 bit	**262k Type A**	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type B	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type C	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	

Remark : x Don't care bits
Not connected pins

ID[1:0]: The address counter is automatically incremented by 1, after data are written to the GDDRAM when ID[1:0] = “1”. The address counter is automatically decremented by 1, after data are written to the GDDRAM when ID[1:0] = “0”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data are written to the GDDRAM is set with AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the GDDRAM. When AM = “0”, the address counter is updated in the horizontal direction. When AM = “1”, the address counter is updated in the vertical direction. When window addresses are selected, data are written to the GDDRAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	I/D[1:0]="00” Horizontal: decrement Vertical: decrement	I/D[1:0]="01” Horizontal: increment Vertical: decrement	I/D[1:0]="10” Horizontal: decrement Vertical: increment	I/D[1:0]="11” Horizontal: increment Vertical: increment
AM="0” Horizontal				
AM="1” Vertical				

LG2–0: Write data to the GDDRAM after comparing the write data written to the GDDRAM by the microcomputer with the values in the compare registers (CPR[5:0], CPG[5:0], CPB[5:0]) and performing a logical and arithmetic operation on them.

Compare register (R04h – R05h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	CPR5	CPR4	CPR3	CPR2	CPR1	CPR0	0	0	CPG5	CPG4	CPG3	CPG2	CPG1	CPG0	0	0
W	1	0	0	0	0	0	0	0	0	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0	0	0

CPR[5:0], CPG[5:0], CPB[5:0]: Set the value for the compare register, of which the data read out from the GDDRAM or data written to the GDDRAM by the microcomputer are compared. This function is not available in the external display interface mode. In the external display mode, make sure LG[2:0] = "000". CPR[5:0] compares the pins RR[5:0], CPG[5:0] compares the pins GG[5:0], and CPB[5:0] compares the pins BB[5:0]. Refer to Section Interface Mapping for writing methods in RGB data.

Display Control (R07h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0

PT[1:0]: Normalize the source outputs when non-displayed area of the partial display is driven.

VLE2–1: When VLE1 = 1 or VLE2 = 1, a vertical scroll is performed in the 1st screen by taking data VL1[7:0] in R41h register. When VLE2 = 1 and VLE1 = 1, a vertical scroll is performed in the 1st and 2nd screen by VL1[7:0] and VL2[7:0] respectively.

SPT: When SPT = "1", the 2-division LCD drive is performed.

CM: When CM = 1, 8-color mode is selected.
Note: Register bit CM will override the CM hardware pin setting.

GON: Gate off level becomes VGH when GON = "0".

DTE: When GON = "1" and DTE = "0", all gate outputs become VGOFFL. When GON = "1" and DTE = "1", selected gate wire becomes VGH, and non-selected gate wires become VGOFFL.

D[1:0]: Display is on when D1 = "1" and off when D1 = "0". When off, the display data remains in the GDDRAM, and can be displayed instantly by setting D1 = "1". When D1= "0", the display is off with all of the source outputs set to the GND level. Because of this, the driver can control the charging current for the LCD with AC driving. When D1–0 = "01", the internal display is performed although the display is off. When D[1:0] = "00", the internal display operation halts and the display is off. Control the display on/off while control GON and DTE.

Table below shows the operation for display

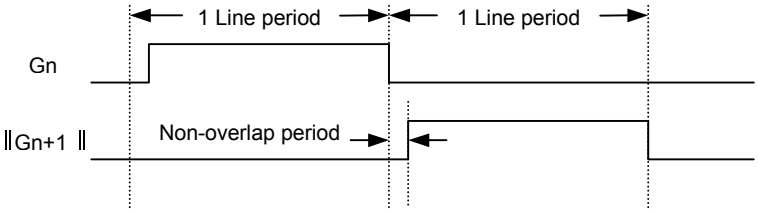
GON	DTE	D1	D0	Internal Display Operation	Source output	Gate output
0	0	0	0	Halt	GND	VGH
0	0	0	1	Operation	GND	VGH
1	0	0	1	Operation	GND	VGOFFL
1	0	1	1	Operation	Grayscale level output	VGOFFL
1	1	1	1	Operation	Grayscale level output	Selected gate line: VGH Non-selected gate line: VGOFFL

Frame Cycle Control (R0Bh) (POR = 5C0Ch)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0

NO[1:0]: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	0 clock cycle
0	1	4 clock cycle
1	0	6 clock cycle
1	1	8 clock cycle

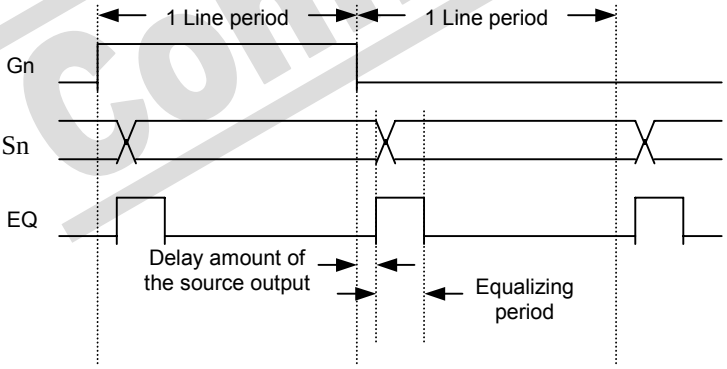


SDT[1:0]: Set delay amount from the gate output signal falling edge of the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	1 clock cycle
0	1	2 clock cycle
1	0	3 clock cycle
1	1	4 clock cycle

EQ[1:0]: Sets the equalizing period.

EQ1	EQ0	EQ period
0	0	No EQ
0	1	1 clock cycle
1	0	2 clock cycle
1	1	3 clock cycle



DIV[1:0]: Set the division ratio of clocks for internal operation. Internal operations are driven by clocks which frequency is divided according to the DIV[1:0] setting.

DIV1	DIV0	Division Ratio $2^{(DIV+1)}$
0	0	2
0	1	4
1	0	8
1	1	16

* fosc = internal oscillator frequency, ~520kHz

SDIV: When SDIV = 1, DIV[1:0] value will be count. When SDIV = 0, DIV[1:0] value will be automatically determined.

SRTN: When SRTN =1, RTN[3:0] value will be count. When SRTN = 0, RTN[3:0] value will be automatically determined.

RTN[3:0]: Set the no. of clocks in each line. The total number will be the decimal value of RTN[3:0] plus 16. e.g. if RTN[3:0] = "1010h", the total number of clocks in each line = 10 +16 = 26 clocks.

Frame frequency calculation

Frame frequency is governed by the below equation, for default setting,

If Dmode[1:0] = "00",

$$Frame\_frequency = \frac{Fosc}{2^{(DIV+1)} \times (rtn+16) \times (mux+vbp+vfp+3)}$$

Fosc = the internal oscillator frequency
DIV = DIV[1:0]
$2^{(DIV+1)}$ = the Division ratio
rtn = RTN[3:0]
mux = MUX[7:0]
vbp = VBP[6:0]
vfp = VFP[6:0]

for default values of SSD1283A,

Fosc ~= 520Khz
MUX[7:0] = 131
VBP[6:0] = 2
VFP[6:0] = 4
RTN[3:0]=12
DIV[1:0]=0:

$$Frame\_frequency = \frac{520kHz}{2 \times 28 \times 140} = 66Hz$$

Power control 1 (R10h) (POR = 2FC5h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DOT	DCY2	DCY1	DCY0	BTH2	BTH1	BTH0	1	1	1	DC1	DC0	AP2	AP1	AP0	SLP

DOT: When DOT = 1, all dcdc clock derivation will use dotclk as clock source Dmode[1:0] = "01", "10" or "11". When DOT=0, all dcdc clock derivation will use onchip oscillator as clock source no matter what Dmode[1:0] is.

DCY[2:0]: Set the step-up cycle of the step-up circuit for high voltage output. When the cycle accelerates, the driving ability of the step-up circuit increases, but its current consumption also increases. Adjust the cycle by taking into account the display quality and the power consumption.

DCY2	DCY1	DCY0	Step-up cycle
0	0	0	Fline x 8
0	0	1	Fline x 4
0	1	0	Fline x 2 (POR if 262k mode)
0	1	1	Fline x 1
1	0	0	fosc / 4
1	0	1	fosc / 8
1	1	0	fosc / 16 (POR if 8 color mode)
1	1	1	fosc / 32

*fosc = internal oscillator frequency
*Fline = line frequency

BTH[2:0]: Control the step-up factor of the step-up circuit on VGH. Adjust the step-up factor according to the power-supply voltage to be used. The voltage selected at BTH[2:0] is limits by the

Note: The voltage selected at BTH[2:0] is limited by the maximum voltage set by the step up multiplying ratio PU[1:0] at R11h. e.g. If VCI = 3.0V and multiplying ratio = x4, the maximum voltage at VGH will be 12V. VGH will be limited to 12V even 13-15V is selected at the BTH register.

BTH2	BTH1	BTH0	VGH output
0	0	0	8V
0	0	1	9V
0	1	0	10V
0	1	1	11V
1	0	0	12V
1	0	1	13V
1	1	0	14V
1	1	1	unregulated

DC[1:0]: Set the step-up cycle of the step-up circuit for VCIX2. When the cycle accelerates, the driving ability of the step-up circuit increases, but its current consumption also increases. Adjust the cycle taking into account the display quality and power consumption.

DC1	DC0	Step-up cycle
0	0	fosc (POR)
0	1	fosc / 2
1	0	fosc /4
1	1	fosc / 8

* fosc = internal oscillator frequency

AP[2:0]: Adjust the amount of current form the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current by taking into account the power consumption. While there is no display, such as the system is in a sleep mode, AP[2:0] can be set to (0,0,0) and shutting down the operational amplifier can reduce the power consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium (POR)
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Maximum
1	1	1	Reserved

SLP: When SLP = 1, the driver enters into the sleep mode. In the sleep mode, the internal display operations are halted except the R-C oscillator to reduce current consumption. Only the power control instructions (R10h – R13h) are executed during the sleep mode. No change in the GDDRAM data or instructions during the sleep mode is made, although it is retained.

Power Control 2 (R11h) (POR = 001Ch)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PU1	PU0	1	0	0

PU[1:0]: Set the step up multiplying ratio of VGH from VCI. This determines the maximum level of VGH.

PU1	PU0	VGH/VCI ratio
0	0	x3
0	1	X4
1	0	X5
1	1	X6 (POR)

Power Control 3 (R12h) (POR = 060Ah)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	1	1	SX263B	V63SH	0	0	0	VRH3	VRH2	VRH1	VRH0

SX263B: When SX263B = 0 will short VCIX2 to VLCD63 during 8 color mode (i.e. CM = 1). When SX263B = 1 will not short VCIX2 to VLCD63

V63SH: Works together with VRH define amplitude magnification of VLCD63 from 1.33 to 2.775 times.

VRH[3:0]: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 1.33 to 2.85 times the voltage set by VRH[3:0].

VRH3	VRH2	VRH1	VRH0	VLCD63 Voltage	
				V63SH=0	V63SH=1
0	0	0	0	Vref x 1.330	
0	0	0	1	Vref x 1.450	
0	0	1	0	Vref x 1.550	
0	0	1	1	Vref x 1.650	
0	1	0	0	Vref x 1.750	
0	1	0	1	Vref x 1.800	
0	1	1	0	Vref x 1.850	
0	1	1	1	Stopped	
1	0	0	0	Vref x 1.900	Vref x 2.03
1	0	0	1	Vref x 2.175	Vref x 2.25
1	0	1	0	Vref x 2.325 (POR)	Vref x 2.40
1	0	1	1	Vref x 2.475	Vref x 2.55
1	1	0	0	Vref x 2.625	
1	1	0	1	Vref x 2.700	
1	1	1	0	Vref x 2.775	
1	1	1	1	Stopped	

*Vref is the internal reference voltage equals to 2.0V.

Power Control 4 (R13h) (POR = 3000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

VcomG: When VcomG = "1", it is possible to set output voltage of VcomL to any level, and the instruction (VDV[4:0]) becomes available. When VcomG = "0", VcomL output is fixed to Hi-z level, VCIM output for VcomL power supply stops, and the instruction (VDV[4:0]) becomes unavailable. Set VcomG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV[4:0]: Set the alternating amplitudes of Vcom at the Vcom alternating drive. These bits amplify 0.54 to 1.17 times the VLCD63 voltage. VCOML is govern by the below equation. When VcomG = "0", the settings become invalid. External voltage at VcomR is referenced when VDV[4:0] = "01111".

VCOML = 0.9475 * VCOMH - VCOMA

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom Amplitude
0	0	0	0	0	VLCD63 x 0.54
0	0	0	0	1	VLCD63 x 0.57
0	0	0	1	0	VLCD63 x 0.60
		:			: Step = 0.03 :
0	1	1	0	1	VLCD63 x 0.93
0	1	1	1	0	VLCD63 x 0.96
0	1	1	1	1	Reference from external variable resistor
1	0	0	0	0	VLCD63 x 0.99
1	0	0	0	1	VLCD63 x 1.02
		:			: Step = 0.03 :
1	0	1	0	1	VLCD63 x 1.14
1	0	1	1	0	VLCD63 x 1.17
1	0	1	1	1	Reserved
1	1	*	*	*	Reserved

Note: Vcom amplitude < 5V

Horizontal Porch (R16h) (POR = 8302h)

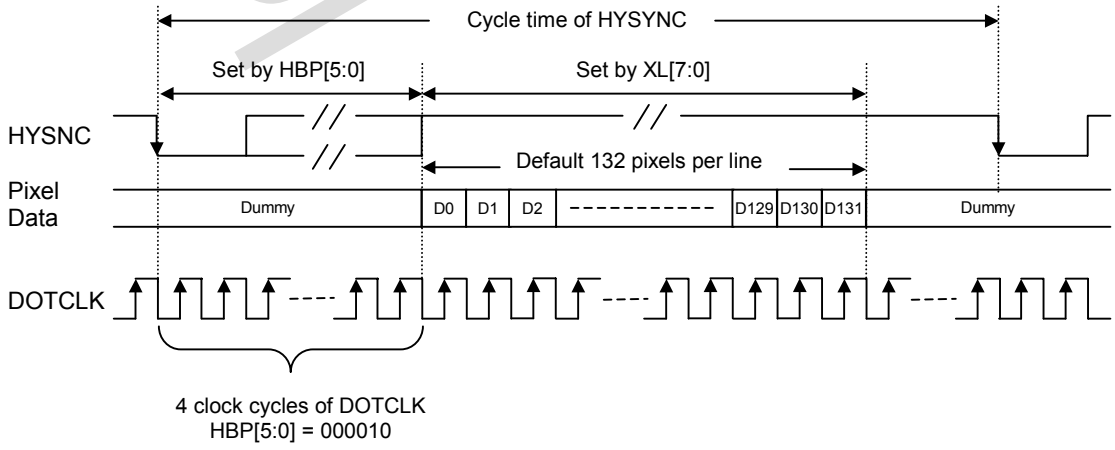
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

XL[7:0]: Set the number of valid pixel per line.

XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	No. of pixel per line
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	: Step = 1 :
1	0	0	0	0	0	1	0	131
1	0	0	0	0	0	1	1	132 (POR)
1	0	0	0	0	1	*	*	Reserved
1	1	*	*	*	*	*	*	Reserved

HBP[5:0]: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XL[7:0] and before the first valid data will be treated as dummy data.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK
0	0	0	0	0	0	2
0	0	0	0	0	1	3
0	0	0	0	1	0	4(POR)
0	0	0	0	1	1	5
0	0	0	1	0	0	6
0	0	0	1	0	1	7
0	0	0	1	1	0	8
0	0	0	1	1	1	9
0	0	1	0	0	0	10
:	:	:	:	:	:	: Step = 1 :
1	1	1	1	1	0	64
1	1	1	1	1	1	65



Vertical Porch (R17h) (POR = 0402h)

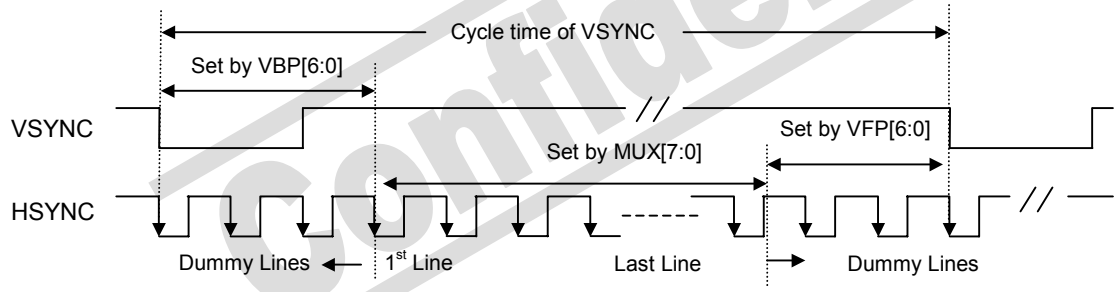
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

VFP[6:0]: Set the delay period from the last valid line to the falling edge of VSYNC of the next frame. The line data within this delay period will be treated as dummy line.

VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
0	0	0	0	0	1	1	4
0	0	0	0	1	0	0	5 (POR)
			:				: Step = 1 :
1	1	1	1	1	1	0	127
1	1	1	1	1	1	1	128

VBP[6:0]: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3 (POR)
0	0	0	0	0	1	1	4
0	0	0	0	1	0	0	5
			:				: Step = 1 :
1	1	1	1	1	1	0	127
1	1	1	1	1	1	1	128



Power Control 5 (R1Eh) (POR = 0036h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

nOTP: nOTP equals to "0" after power on reset and VcomH voltage equals to programmed OTP register(OTPR) value XOR with VCMR. When nOTP set to "1", setting of VCM[5:0] becomes valid and voltage of VcomH can be adjusted regardless VCMR[5:0] values.

VCM[5:0]: To set the VcomH voltage if nOTP = "1". These bits amplify the VcomH voltage 0.36 to 0.99 times the VLCD63 voltage. Default value is "101000" when power on reset.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VcomH
0	0	0	0	0	0	VLCD63 x 0.36
0	0	0	0	0	1	VLCD63 x 0.37
:			Step = 0.01		:	
1	1	1	1	1	0	VLCD63 x 0.98
1	1	1	1	1	1	VLCD63 x 0.99

Please refer to R1Fh for further detail

Power Control 6 (R1Fh) (POR = 0036h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	VCMR5	VCMR4	VCMR3	VCMR2	VCMR1	VCMR0

VCMR[5:0]: To set the VcomH default voltage if nOTP = "0". These bits amplify the VcomH voltage 0.36 to 0.99 times the VLCD63 voltage. Default value is "110110" when power on reset.

VCMR5 XOR OTPR5	VCMR4 XOR OTPR 4	VCMR3 XOR OTPR 3	VCMR2 XOR OTPR 2	VCMR1 XOR OTPR 1	VCMR0 XOR OTPR 0	VcomH
0	0	0	0	0	0	VLCD63 x 0.36
0	0	0	0	0	1	VLCD63 x 0.37
:			Step = 0.01		:	
1	1	1	1	1	0	VLCD63 x 0.98
1	1	1	1	1	1	VLCD63 x 0.99

Note: 2V < VcomH < VCIx2
*** XOR means exclusive or**

OTPR[5:0] are the OTP registers correspondingly

Please refer to OTP detail for more detail

RAM address set (R21h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

AD15–0: Make initial settings for the GDDRAM address in the address counter (AC). After GRAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and setting for a new GDDRAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address counter is not automatically updated when data are read out from the GDDRAM.

GDDRAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses.

Write Data to GRAM (R22h)

R/W	DC	D[17:0]
W	1	WD[17:0] mapping depends on the interface setting

WD17–0: Transforms all the GDDRAM data into 18-bit, and writes the data. Format for transforming data into 18-bit depends on the interface used. SSD1283A selects the grayscale level according to the GDDRAM data. After writing data to GDDRAM, address is automatically updated according to AM bit and ID bit. Access to GDDRAM during stand-by mode is not available.

Read Data from GRAM (R22h)

R/W	DC	D[17:0]
R	1	RD[17:0] mapping depends on the interface setting

RD17–0: Read 18-bit data from the GDDRAM. When the data is read to the microcomputer, the first-word read immediately after the GDDRAM address setting is latched from the GDDRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed, only one read can be processed since the latched data in the first word is used.

RAM write data mask (R23h – R24h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WMR5	WMR4	WMR3	WMR2	WMR1	WMR0	0	0	WMG5	WMG4	WMG3	WMG2	WMG1	WMG0	0	0
W	1	0	0	0	0	0	0	0	0	WMB5	WMB4	WMB3	WMB2	WMB1	WMB0	0	0

WMR[5:0], WMG[5:0], WMB[5:0]: In writing to the GDDRAM, these bits write-mask the data to be written to the GDDRAM by a bit unit. For example, if WMR5 = 1, the WMR5 write-mask is enabled and data RR5 will be masked and not write into the GDDRAM. WMR[5:0] mask pins RR[5:0], WMG[5:0] mask pins GG[5:0], and WMB[5:0] mask pins BB[5:0]. For writing GDDRAM methods, refer to Section Interface Mapping".

Vcom OTP (R28h – R29h)

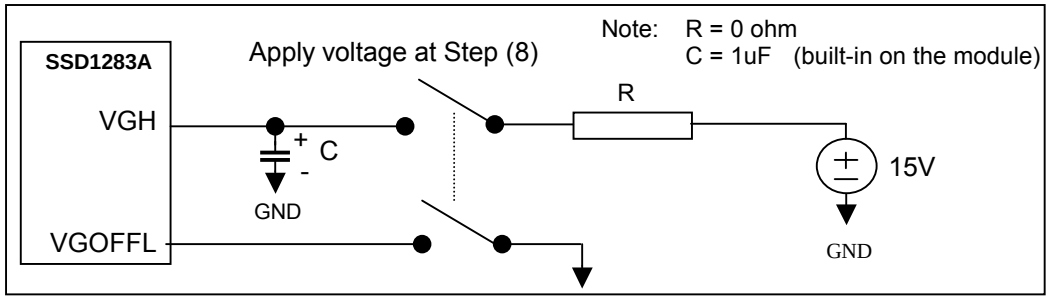
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
W	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

When OTP is access, these registers must be set accordantly.

OTP programming sequence

Step	Operation
1	Power up the module at VCI = 2.7V, VDD = VDDIO = 1.8V. Turn on the display as normal to 65k/262k color mode (displaying a test pattern if any).
2	Set VCMR value by adjusting (R1Fh). Set nOTP to "1" (R1Eh) and optimizes VcomH by adjusting VCM[5:0] (R1Eh).
3	Insert the below commands Index / Value R28h 0x0006 R29h 0x8000 R27h 0x0578 R29h 0x89A1
4	Wait 300ms
5	Power down the whole module.
6	Connect a power supply to the module at VCI = 3.0V, VDD = VDDIO = 1.8V.
7	Write below commands for OTP initialization and wait for 200ms for activate the OTP : Index / Value R00h 0x0001 R28h 0x0006 R29h 0x80C0 R10h 0x2FC0 R07h 0x0033 R2Bh 0x1A81
8	Connect a power supply to the module at VGH = 15.0V and connect VGOFFL to VSS.
9	Write the optimized value found in Step 2 to VCM[5:0] (R1Eh) and set nOTP to "1".
10	Fire the OTP by write HEX code "000Ah" to register R28h.
11	Wait at least 3 seconds.
12	OTP complete. Power down the whole module and remove 15V supply.

Note: nOTP must set to "0" to activate the OTP effect.



Gamma Control (R30h to R39h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

PKP52–00: Gamma micro adjustment register for the positive polarity output

PRP12-00: Gradient adjustment register for the positive polarity output

VRP14-00: Adjustment register for amplification adjustment of the positive polarity output

PKN52-00: Gamma micro adjustment register for the negative polarity output

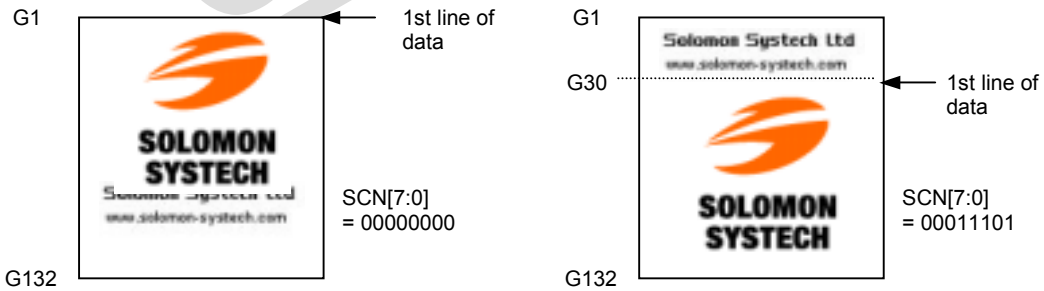
PRN12-00: Gradient adjustment register for the negative polarity output

VRN14-00: Adjustment register for the amplification adjustment of the negative polarity output.
(For details, see the Section Gamma Adjustment Function).

Gate Scan Position (R40h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN[7:0]: Set the scanning starting position of the gate driver. The valid range is from 0 to 131.



Vertical Scroll Control (R41h) (POR =0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10

VL2[7:0]: Specify scroll length at the scroll display for vertical smooth scrolling at 2nd screen. The display-start raster-row (VL2[7:0]) is valid when VLE1 = "1" and VLE2 = "1".

VL1[7:0]: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 132nd can be scrolled for the number of the raster-row. After 132nd raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL1[7:0]) is valid when VLE1 = "1" or VLE2 = "1". The raster-row display is fixed when VLE2-1 = "00".

1st Screen driving position (R42h) (POR = 8300h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

SS1[7:0]: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the set value + 1 gate driver.

SE1[7:0]: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the set value + 1 gate driver. For instance, when SS17–10 = "07"H and SE17–10 = "10"H are set, the LCD driving is performed from G8 to G17, and non-selection driving is performed for G1 to G7, G18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ 83H.

2nd Screen driving position (R43h) (POR = 8300h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS2[7:0]: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the set value + 1 gate driver. The second screen is driven when SPT = "1".

SE2[7:0]: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the set value + 1 gate driver. For instance, when SPT = "1", SS27–20 = "20"H, and SE27–20 = "2F"H are set, the LCD driving is performed from G33 to G48. Ensure that SS17–10 ≤ SE17–10; SS27–20 ≤ SE27–20 ≤ 83H.

Horizontal RAM address position (R44h) (POR = 8300h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

HSA[7:0]/HEA[7:0]: Specify the start/end positions of the window address in the horizontal direction by an address unit. Data are written to the GDDRAM within the area determined by the addresses specified by HEA[7:0] and HSA[7:0]. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ HSA[7:0] ≤ HEA[7:0] ≤ "83"h.

Vertical RAM address position (R45h) (POR = 8300h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

VSA[7:0]/VEA[7:0]: Specify the start/end positions of the window address in the vertical direction by an address unit. Data are written to the GRAM within the area determined by the addresses specified by VEA[7:0] and VSA[7:0]. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ VSA[7:0] ≤ VEA[7:0] ≤ "83"h.

10 Extended command description

Further bias current setting (R27h) (POR = 0540h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	1	0	1	0	1	IU2	IU1	IU0	0	0	0

IU2	IU1	IU0	Bias current
0	0	0	Least (POR)
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Maximum
1	1	1	Reserved

Oscillator frequency (R2Ch) (POR = 8000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	OSCR3	OSCR2	OSCR1	OSCR0	0	0	0	0	0	0	0	0	0	0	0	0

OSCR[3:0]: To set the oscillator frequency.

OSCR3	OSCR2	OSCR1	OSCR0	Oscillator frequency (kHz)
1	0	0	0	520
Other settings				Reserved

11 Gamma Adjustment Function

The SSD1283A incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

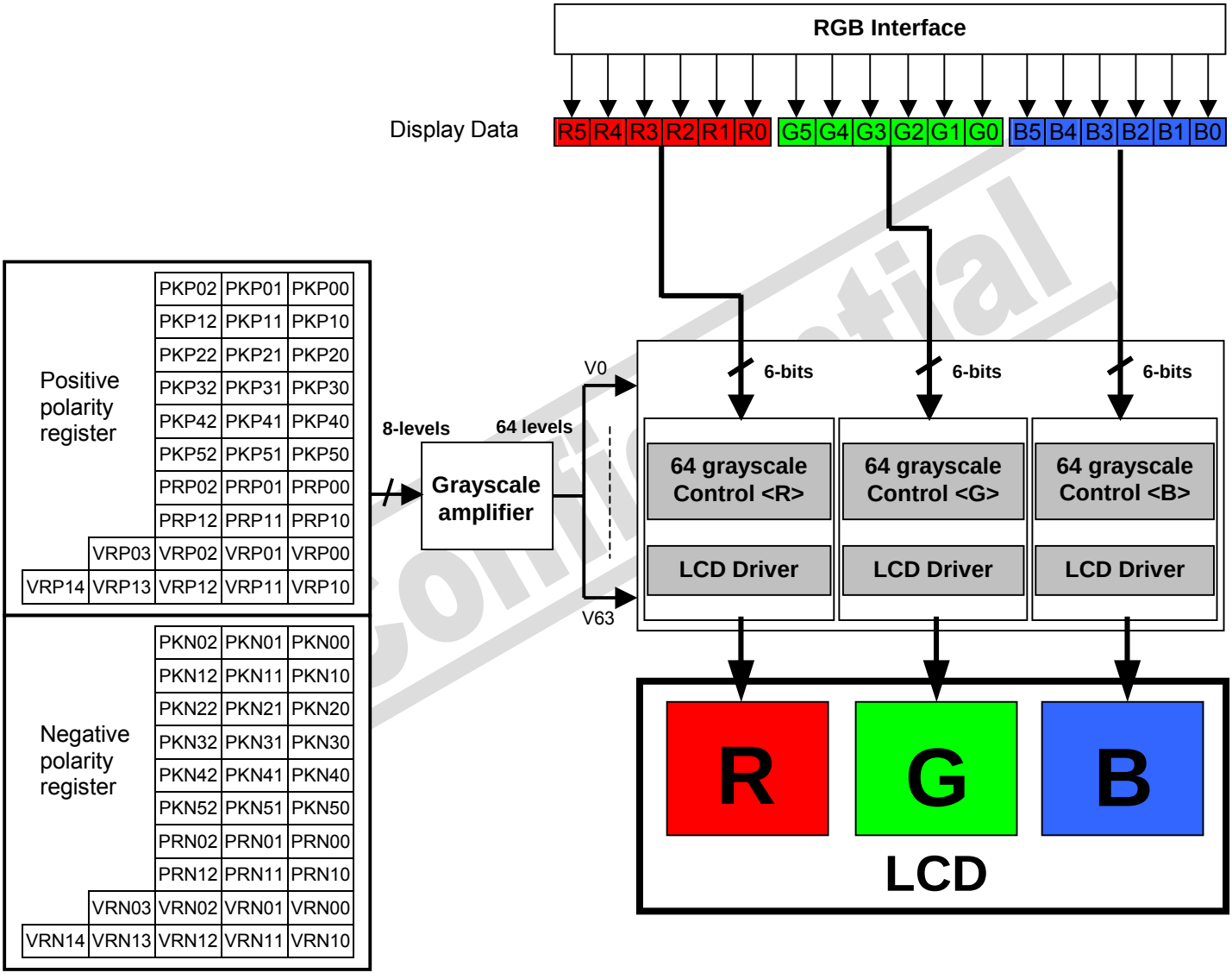


Figure 4 - Grayscale Control Block

11.1 Structure of Grayscale Amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.

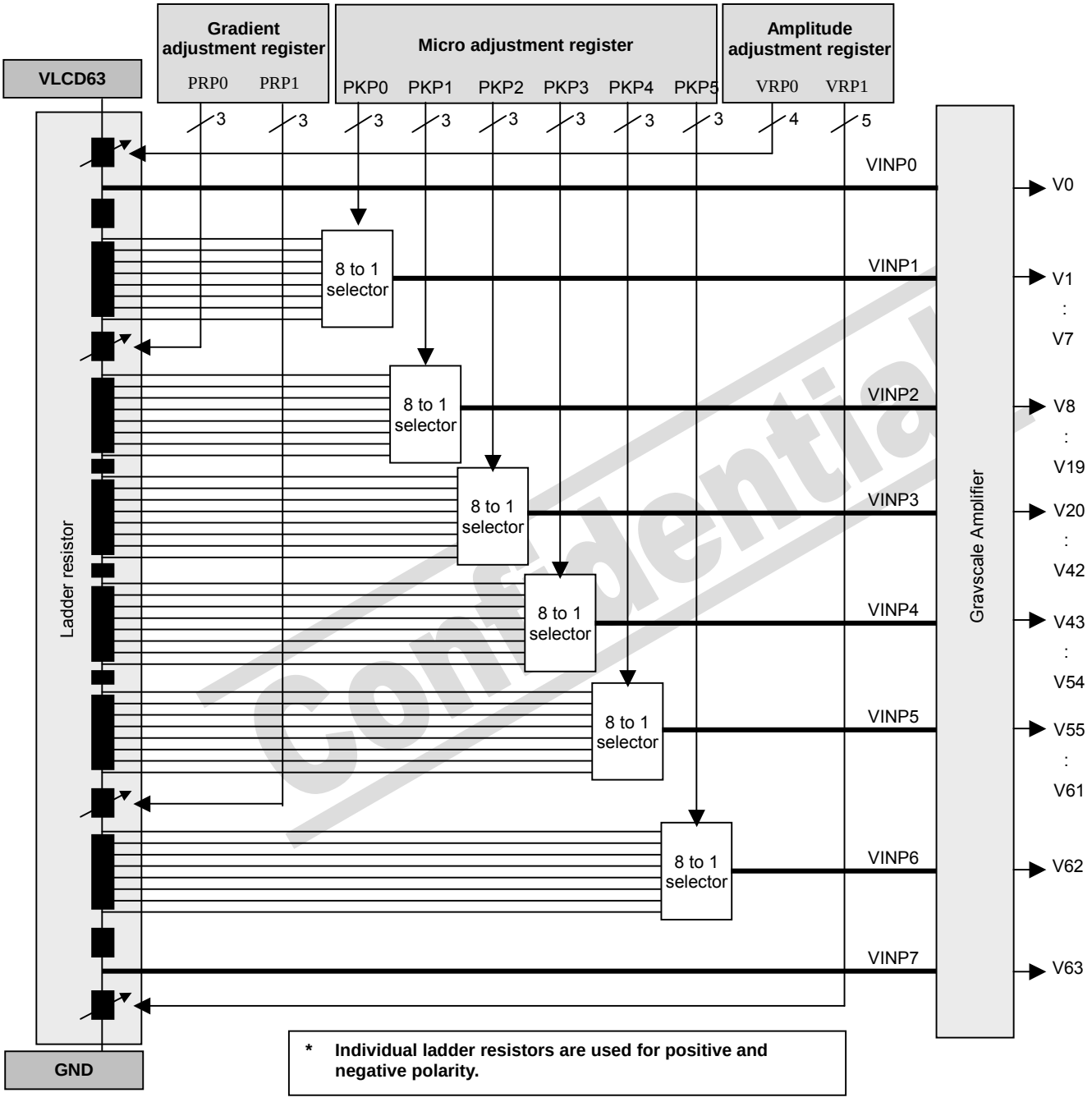


Figure 5 - Grayscale Amplifier

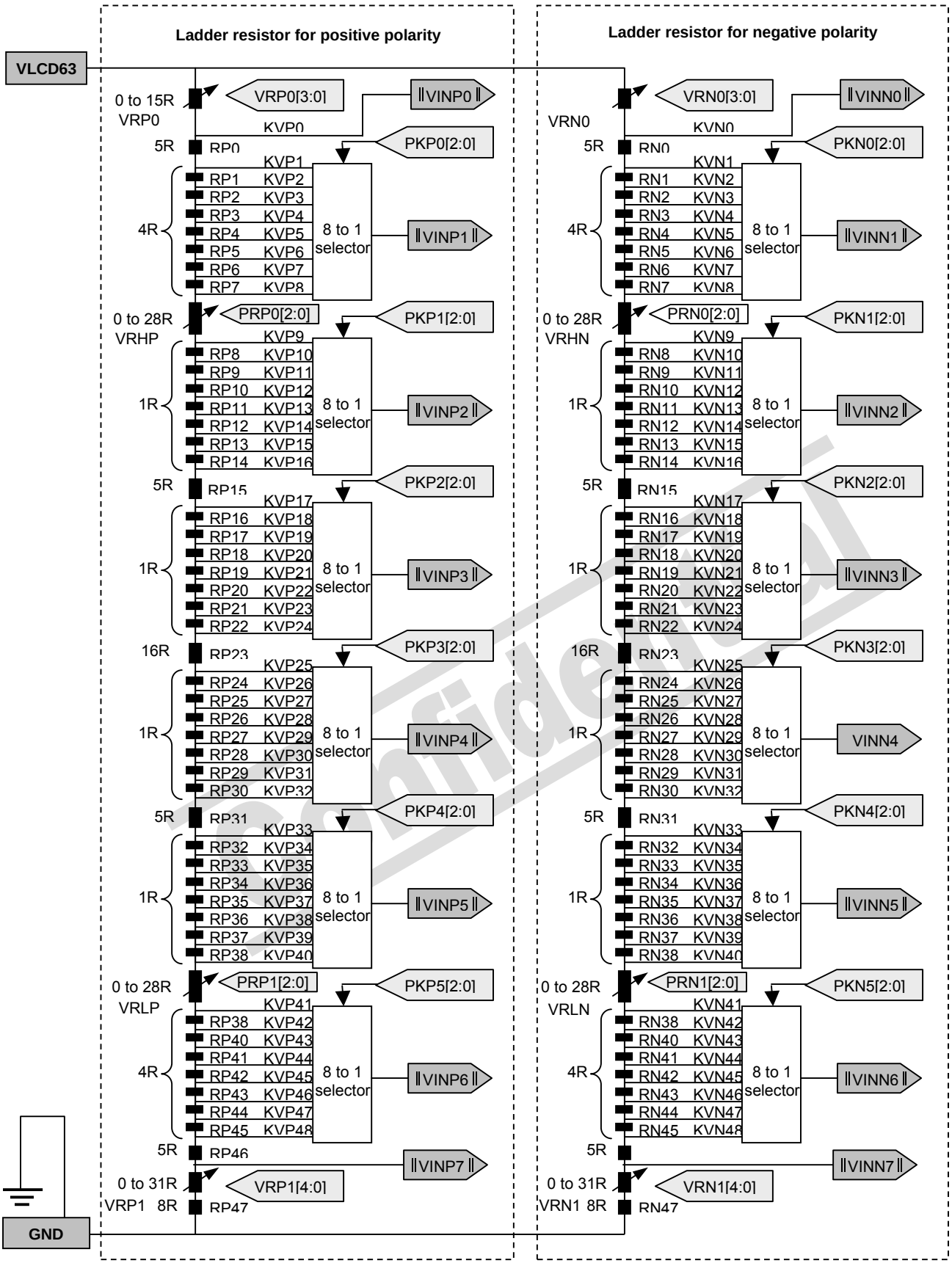


Figure 6 - Resistor Ladder for Gamma Voltages Generation

11.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.

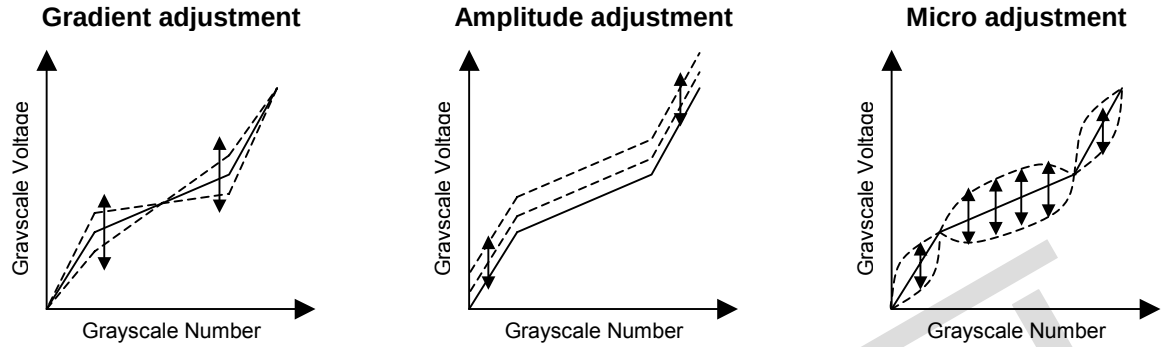


Figure 7 - Gamma Adjustment Function

11.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

11.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

11.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

11.3 Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

VRP(N)0	Resistance
0000	0R
0001	1R
0010	2R
: Step = 1R :	
1110	14R
1111	15R

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
: Step = 1R :	
11110	30R
11111	31R

8 to 1 selecter

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Postive polarity							Negative polarity						
Registor	Selected voltage						Registor	Selected voltage					
PKP[2:0]	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6	PKN[2:0]	VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Grayscale voltage	Formula	Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP(N)0	V22	V43+(V20-V43)*(21/23)	V44	V55+(V43-V55)*(22/24)
V1	VINP(N)1	V23	V43+(V20-V43)*(20/23)	V45	V55+(V43-V55)*(20/24)
V2	V8+(V1-V8)*(30/48)	V24	V43+(V20-V43)*(19/23)	V46	V55+(V43-V55)*(18/24)
V3	V8+(V1-V8)*(23/48)	V25	V43+(V20-V43)*(18/23)	V47	V55+(V43-V55)*(16/24)
V4	V8+(V1-V8)*(16/48)	V26	V43+(V20-V43)*(17/23)	V48	V55+(V43-V55)*(14/24)
V5	V8+(V1-V8)*(12/48)	V27	V43+(V20-V43)*(16/23)	V49	V55+(V43-V55)*(12/24)
V6	V8+(V1-V8)*(8/48)	V28	V43+(V20-V43)*(15/23)	V50	V55+(V43-V55)*(10/24)
V7	V8+(V1-V8)*(4/48)	V29	V43+(V20-V43)*(14/23)	V51	V55+(V43-V55)*(8/24)
V8	VINP(N)2	V30	V43+(V20-V43)*(13/23)	V52	V55+(V43-V55)*(6/24)
V9	V20+(V8-V20)*(22/24)	V31	V43+(V20-V43)*(12/23)	V53	V55+(V43-V55)*(4/24)
V10	V20+(V8-V20)*(20/24)	V32	V43+(V20-V43)*(11/23)	V54	V55+(V43-V55)*(2/24)
V11	V20+(V8-V20)*(18/24)	V33	V43+(V20-V43)*(10/23)	V55	VINP(N)5
V12	V20+(V8-V20)*(16/24)	V34	V43+(V20-V43)*(9/23)	V56	V62+(V55-V62)*(44/48)
V13	V20+(V8-V20)*(14/24)	V35	V43+(V20-V43)*(8/23)	V57	V62+(V55-V62)*(40/48)
V14	V20+(V8-V20)*(12/24)	V36	V43+(V20-V43)*(7/23)	V58	V62+(V55-V62)*(36/48)
V15	V20+(V8-V20)*(10/24)	V37	V43+(V20-V43)*(6/23)	V59	V62+(V55-V62)*(32/48)
V16	V20+(V8-V20)*(8/24)	V38	V43+(V20-V43)*(5/23)	V60	V62+(V55-V62)*(25/48)
V17	V20+(V8-V20)*(6/24)	V39	V43+(V20-V43)*(4/23)	V61	V62+(V55-V62)*(18/48)
V18	V20+(V8-V20)*(4/24)	V40	V43+(V20-V43)*(3/23)	V62	VINP(N)6
V19	V20+(V8-V20)*(2/24)	V41	V43+(V20-V43)*(2/23)	V63	VINP(N)7
V20	VINP(N)3	V42	V43+(V20-V43)*(1/23)		
V21	V43+(V20-V43)*(22/23)	V43	VINP(N)4		

Reference voltage of positive polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVP0	VLCD63 - ΔV x VRP0 / SUMRP	--	VINP0
KVP1	VLCD63 - ΔV x (VRP0 + 5R) / SUMRP	PKP0[2:0] = “000”	VINP1
KVP2	VLCD63 - ΔV x (VRP0 + 9R) / SUMRP	PKP0[2:0] = “001”	
KVP3	VLCD63 - ΔV x (VRP0 + 13R) / SUMRP	PKP0[2:0] = “010”	
KVP4	VLCD63 - ΔV x (VRP0 + 17R) / SUMRP	PKP0[2:0] = “011”	
KVP5	VLCD63 - ΔV x (VRP0 + 21R) / SUMRP	PKP0[2:0] = “100”	
KVP6	VLCD63 - ΔV x (VRP0 + 25R) / SUMRP	PKP0[2:0] = “101”	
KVP7	VLCD63 - ΔV x (VRP0 + 29R) / SUMRP	PKP0[2:0] = “110”	
KVP8	VLCD63 - ΔV x (VRP0 + 33R) / SUMRP	PKP0[2:0] = “111”	
KVP9	VLCD63 - ΔV x (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = “000”	VINP2
KVP10	VLCD63 - ΔV x (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = “001”	
KVP11	VLCD63 - ΔV x (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = “010”	
KVP12	VLCD63 - ΔV x (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = “011”	
KVP13	VLCD63 - ΔV x (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = “100”	
KVP14	VLCD63 - ΔV x (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = “101”	
KVP15	VLCD63 - ΔV x (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = “110”	
KVP16	VLCD63 - ΔV x (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = “111”	
KVP17	VLCD63 - ΔV x (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = “000”	VINP3
KVP18	VLCD63 - ΔV x (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = “001”	
KVP19	VLCD63 - ΔV x (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = “010”	
KVP20	VLCD63 - ΔV x (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = “011”	
KVP21	VLCD63 - ΔV x (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = “100”	
KVP22	VLCD63 - ΔV x (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = “101”	
KVP23	VLCD63 - ΔV x (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = “110”	
KVP24	VLCD63 - ΔV x (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = “111”	
KVP25	VLCD63 - ΔV x (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = “000”	VINP4
KVP26	VLCD63 - ΔV x (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = “001”	
KVP27	VLCD63 - ΔV x (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = “010”	
KVP28	VLCD63 - ΔV x (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = “011”	
KVP29	VLCD63 - ΔV x (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = “100”	
KVP30	VLCD63 - ΔV x (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = “101”	
KVP31	VLCD63 - ΔV x (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = “110”	
KVP32	VLCD63 - ΔV x (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = “111”	
KVP33	VLCD63 - ΔV x (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = “000”	VINP5
KVP34	VLCD63 - ΔV x (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = “001”	
KVP35	VLCD63 - ΔV x (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = “010”	
KVP36	VLCD63 - ΔV x (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = “011”	
KVP37	VLCD63 - ΔV x (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = “100”	
KVP38	VLCD63 - ΔV x (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = “101”	
KVP39	VLCD63 - ΔV x (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = “110”	
KVP40	VLCD63 - ΔV x (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = “111”	
KVP41	VLCD63 - ΔV x (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “000”	VINP6
KVP42	VLCD63 - ΔV x (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “001”	
KVP43	VLCD63 - ΔV x (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “010”	
KVP44	VLCD63 - ΔV x (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “011”	
KVP45	VLCD63 - ΔV x (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “100”	
KVP46	VLCD63 - ΔV x (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “101”	
KVP47	VLCD63-ΔV x (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “110”	
KVP48	VLCD63 - ΔV x (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “111”	
KVP49	VLCD63 - ΔV x (VRP0 + 120R + VRHP + VRLP) / SUMRP	--	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1
ΔV: Voltage difference between VLCD63 and of GND.

Reference voltage of negative polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVN0	VLCD63 - ΔV x VRN0 / SUMRN	--	VINN0
KVN1	VLCD63 - ΔV x (VRN0 + 5R) / SUMRN	PKN0[2:0] = “000”	VINN1
KVN2	VLCD63 - ΔV x (VRN0 + 9R) / SUMRN	PKN0[2:0] = “001”	
KVN3	VLCD63 - ΔV x (VRN0 + 13R) / SUMRN	PKN0[2:0] = “010”	
KVN4	VLCD63 - ΔV x (VRN0 + 17R) / SUMRN	PKN0[2:0] = “011”	
KVN5	VLCD63 - ΔV x (VRN0 + 21R) / SUMRN	PKN0[2:0] = “100”	
KVN6	VLCD63 - ΔV x (VRN0 + 25R) / SUMRN	PKN0[2:0] = “101”	
KVN7	VLCD63 - ΔV x (VRN0 + 29R) / SUMRN	PKN0[2:0] = “110”	
KVN8	VLCD63 - ΔV x (VRN0 + 33R) / SUMRN	PKN0[2:0] = “111”	
KVN9	VLCD63 - ΔV x (VRN0 + 33R + VRHN) / SUMRN	PKN1[2:0] = “000”	VINN2
KVN10	VLCD63 - ΔV x (VRN0 + 34R + VRHN) / SUMRN	PKN1[2:0] = “001”	
KVN11	VLCD63 - ΔV x (VRN0 + 35R + VRHN) / SUMRN	PKN1[2:0] = “010”	
KVN12	VLCD63 - ΔV x (VRN0 + 36R + VRHN) / SUMRN	PKN1[2:0] = “011”	
KVN13	VLCD63 - ΔV x (VRN0 + 37R + VRHN) / SUMRN	PKN1[2:0] = “100”	
KVN14	VLCD63 - ΔV x (VRN0 + 38R + VRHN) / SUMRN	PKN1[2:0] = “101”	
KVN15	VLCD63 - ΔV x (VRN0 + 39R + VRHN) / SUMRN	PKN1[2:0] = “110”	
KVN16	VLCD63 - ΔV x (VRN0 + 40R + VRHN) / SUMRN	PKN1[2:0] = “111”	
KVN17	VLCD63 - ΔV x (VRN0 + 45R + VRHN) / SUMRN	PKN2[2:0] = “000”	VINN3
KVN18	VLCD63 - ΔV x (VRN0 + 46R + VRHN) / SUMRN	PKN2[2:0] = “001”	
KVN19	VLCD63 - ΔV x (VRN0 + 47R + VRHN) / SUMRN	PKN2[2:0] = “010”	
KVN20	VLCD63 - ΔV x (VRN0 + 48R + VRHN) / SUMRN	PKN2[2:0] = “011”	
KVN21	VLCD63 - ΔV x (VRN0 + 49R + VRHN) / SUMRN	PKN2[2:0] = “100”	
KVN22	VLCD63 - ΔV x (VRN0 + 50R + VRHN) / SUMRN	PKN2[2:0] = “101”	
KVN23	VLCD63 - ΔV x (VRN0 + 51R + VRHN) / SUMRN	PKN2[2:0] = “110”	
KVN24	VLCD63 - ΔV x (VRN0 + 52R + VRHN) / SUMRN	PKN2[2:0] = “111”	
KVN25	VLCD63 - ΔV x (VRN0 + 68R + VRHN) / SUMRN	PKN3[2:0] = “000”	VINN4
KVN26	VLCD63 - ΔV x (VRN0 + 69R + VRHN) / SUMRN	PKN3[2:0] = “001”	
KVN27	VLCD63 - ΔV x (VRN0 + 70R + VRHN) / SUMRN	PKN3[2:0] = “010”	
KVN28	VLCD63 - ΔV x (VRN0 + 71R + VRHN) / SUMRN	PKN3[2:0] = “011”	
KVN29	VLCD63 - ΔV x (VRN0 + 72R + VRHN) / SUMRN	PKN3[2:0] = “100”	
KVN30	VLCD63 - ΔV x (VRN0 + 73R + VRHN) / SUMRN	PKN3[2:0] = “101”	
KVN31	VLCD63 - ΔV x (VRN0 + 74R + VRHN) / SUMRN	PKN3[2:0] = “110”	
KVN32	VLCD63 - ΔV x (VRN0 + 75R + VRHN) / SUMRN	PKN3[2:0] = “111”	
KVN33	VLCD63 - ΔV x (VRN0 + 80R + VRHN) / SUMRN	PKN4[2:0] = “000”	VINN5
KVN34	VLCD63 - ΔV x (VRN0 + 81R + VRHN) / SUMRN	PKN4[2:0] = “001”	
KVN35	VLCD63 - ΔV x (VRN0 + 82R + VRHN) / SUMRN	PKN4[2:0] = “010”	
KVN36	VLCD63 - ΔV x (VRN0 + 83R + VRHN) / SUMRN	PKN4[2:0] = “011”	
KVN37	VLCD63 - ΔV x (VRN0 + 84R + VRHN) / SUMRN	PKN4[2:0] = “100”	
KVN38	VLCD63 - ΔV x (VRN0 + 85R + VRHN) / SUMRN	PKN4[2:0] = “101”	
KVN39	VLCD63 - ΔV x (VRN0 + 86R + VRHN) / SUMRN	PKN4[2:0] = “110”	
KVN40	VLCD63 - ΔV x (VRN0 + 87R + VRHN) / SUMRN	PKN4[2:0] = “111”	
KVN41	VLCD63 - ΔV x (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “000”	VINN6
KVN42	VLCD63 - ΔV x (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “001”	
KVN43	VLCD63 - ΔV x (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “010”	
KVN44	VLCD63 - ΔV x (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “011”	
KVN45	VLCD63 - ΔV x (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “100”	
KVN46	VLCD63 - ΔV x (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “101”	
KVN47	VLCD63-ΔV x (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “110”	
KVN48	VLCD63 - ΔV x (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “111”	
KVN49	VLCD63 - ΔV x (VRN0 + 120R + VRHN + VRLN) / SUMRN	--	VINN7

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1

ΔV: Voltage difference between VLCD63 and of GND.

12 MAXIMUM RATINGS

Table 6 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
VDD	Supply Voltage	-0.3 to +2.7	V
VDDIO		-0.3 to +4.0	V
VDDEXT		-0.3 to +4.0	V
VCI	Input Voltage	VSS - 0.3 to 5.0	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-20 to +70	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC
Ron	Input Resistance	TBD	Ω

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and Vout be constrained to the range VSS < VDDIO ≤ VCI < V_{OUT}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

13 DC CHARACTERISTICS

Table 7 - DC Characteristics

(Unless otherwise specified, Voltage Referenced to VSS, VDDIO = 2.5 to 3.6V, VCI = 2.5 to 3.6V, TA = -20 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	System power supply pins of the logic block	Recommend Operating Voltage Possible Operating Voltage	1.65	-	2.5	V
V_{DDIO}	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.6	V
V_{DDEXT}	Auxiliary power supply pin for VDD	Recommend Operating Voltage Possible Operating Voltage	1.65	-	3.6	V
V_{CI}	Booster Reference Supply Voltage Range (3)	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO	-	3.6	V
V_{GH}	Gate driver High Output Voltage Booster efficiency[1]	No panel loading; 4x booster; ITO for VCIX2, VCI and VCHS = 10 Ohm	82	89.5	-	%
		No panel loading; 5x booster; ITO for VCIX2, VCI and VCHS = 10 Ohm	78	88.5	-	%
		No panel loading; 6x booster; ITO for VCIX2, VCI and VCHS = 10 Ohm	70	80	-	%
V_{CIX2}	VCIX2 primary booster efficiency[2]	No panel loading, 4x or 5x booster; ITO for VCIX2, VCI and VCHS = 10 Ohm	83	90	-	%
V_{goffL}	Gate driver Low Output Voltage		-15.0	-	-	V
V_{comH}	Vcom High Output Voltage			TBD		
V_{comL}	Vcom Low Output Voltage		VCIM+0.5	TBD		V
V_{LCD63}	Max. Source Voltage		-	-	V_{CIX2}-0.1	V
ΔV_{LCD63}	Source voltage variation		-2		2	%
V_{OH1}	Logic High Output Voltage	Iout=-100μA	0.9* VDDIO	-	VDDIO	V
V_{OL1}	Logic Low Output Voltage	Iout=100μA	0	-	0.1*VDDIO	V
V_{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I_{OH}	Logic High Output Current Source	Vout = V_{DD}-0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	μA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
F_{FRAME}	Frame frequency	Display is ON	60	66	70	Hz
f_{OSC}	Internal oscillator frequency variation		-10	-	10	%
TC	Temperature compensation		-	TBD	-	%
I_{dp}(262k)	VCI display current at 262k mode	Full color current consumption without panel loading	-	2.4	-	mA
I_{dp}(8 color)	VCI display current at 8 color mode	8 color mode current consumption without panel loading	-	600	-	μA
I_{slp}	VCI sleep mode current	Oscillator off, no source/gate output, ram read write halt	-	70	-	μA
R_{SON}	Source drivers output resistance		-	1	TBD	kΩ
R_{GON}	Gate drivers output resistance		-	500	TBD	Ω
R_{CON}	Vcom output resistance		-	200	TBD	Ω

Note1: VGH efficiency = VGH/(VCI x n) x 100% (where n = booster factor)
Note2: VCIX2 efficiency = VCIX2 /(VCI x2) x 100%

14 AC CHARACTERISTICS

Table 8 - Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	66	100	-	ns
t_{AS}	Address Setup Time	-	TBD	-	ns
t_{AH}	Address Hold Time	-	TBD	-	ns
t_{DSW}	Data Setup Time	-	TBD	-	ns
t_{DHW}	Data Hold Time	-	TBD	-	ns
t_{ACC}	Data Access Time	-	TBD	-	ns
t_{OH}	Output Hold time	-	TBD	-	ns
PW_{CSH}	Chip Select High Pulse Width (write cycle)	-	TBD	-	ns
PW_{CSL}	Chip Select Low Pulse Width (write cycle)	-	TBD	-	ns
t_F	Chip Select Fall Time	-	TBD	-	ns
t_R	Chip Select Rise Time	-	TBD	-	ns

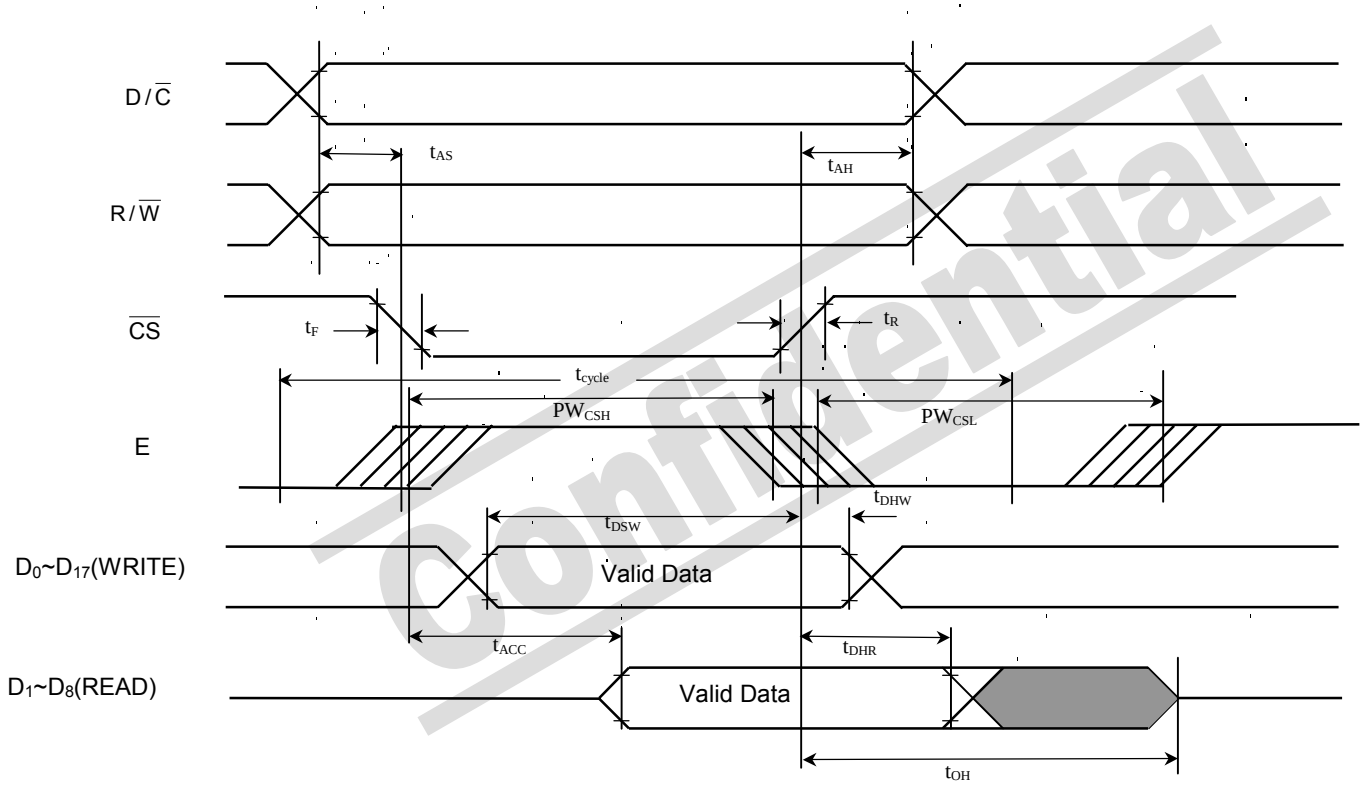


Figure 8 - Parallel 6800-series Interface Timing Characteristics

Table 9 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.6V to 3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	-	TBD	-	ns
t_{AS}	Address Setup Time	-	TBD	-	ns
t_{AH}	Address Hold Time	-	TBD	-	ns
t_{DSW}	Data Setup Time	-	TBD	-	ns
t_{DHW}	Data Hold Time	-	TBD	-	ns
t_{ACC}	Data Access Time	-	TBD	-	ns
t_{OH}	Output Hold time	-	TBD	-	ns
PW_{CSH}	Chip Select High Pulse Width (write cycle)	-	TBD	-	ns
PW_{CSL}	Chip Select Low Pulse Width (write cycle)	-	TBD	-	ns
t_F	Chip Select Fall Time	-	TBD	-	ns
t_R	Chip Select Rise Time	-	TBD	-	ns

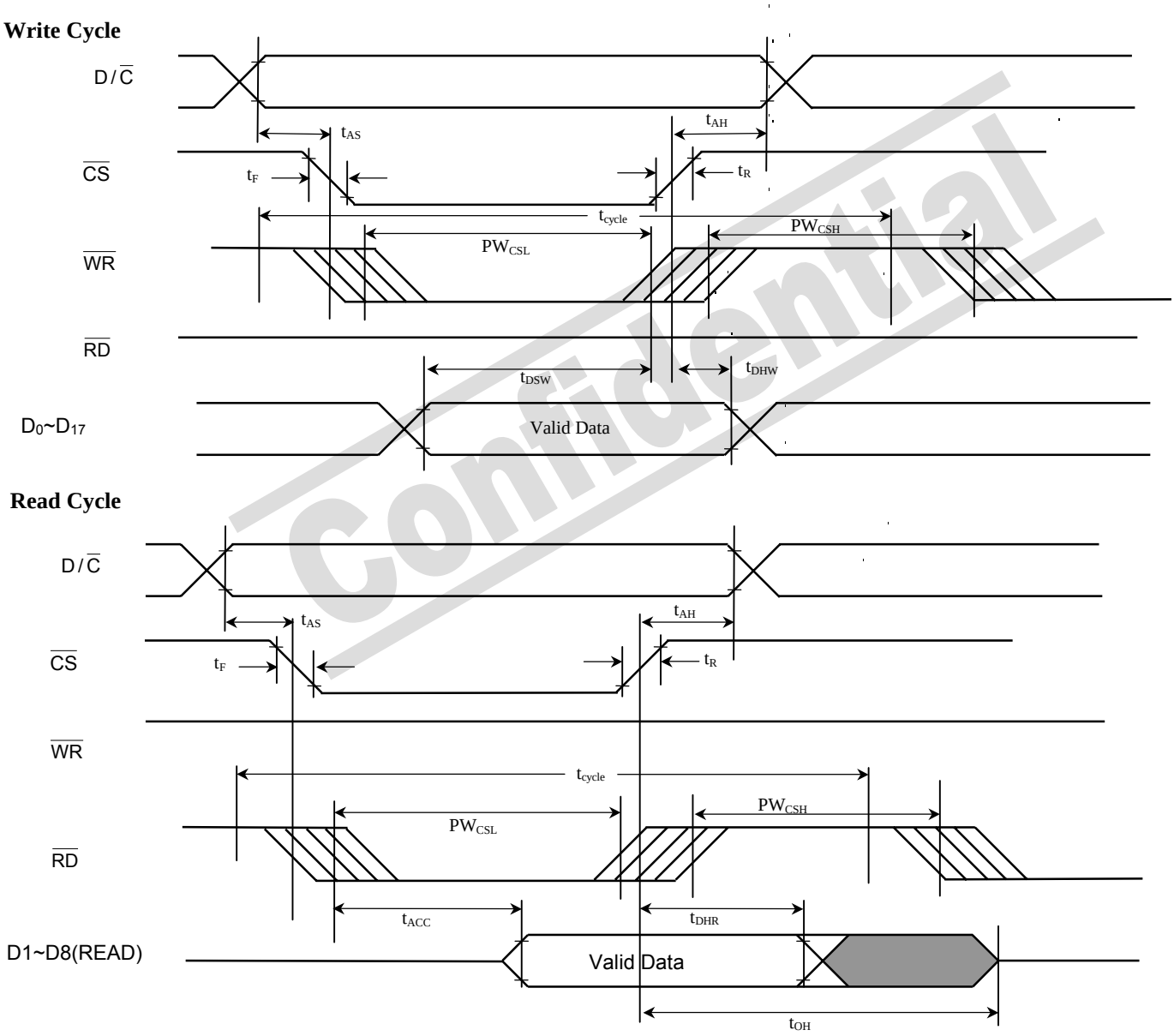


Figure 9 - Parallel 8080-series Interface Timing Characteristics

Table 10 - Serial Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	-	TBD	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	TBD	-	MHz
t_{AS}	Register select Setup Time	-	TBD	-	ns
t_{AH}	Register select Hold Time	-	TBD	-	ns
t_{CSS}	Chip Select Setup Time	-	TBD	-	ns
t_{CSH}	Chip Select Hold Time	-	TBD	-	ns
t_{DSW}	Write Data Setup Time	-	TBD	-	ns
t_{OHW}	Write Data Hold Time	-	TBD	-	ns
t_{CLKL}	Clock Low Time	-	TBD	-	ns
t_{CLKH}	Clock High Time	-	TBD	-	ns
t_F	Chip Select Fall Time	-	TBD	-	ns
t_R	Chip Select Rise Time	-	TBD	-	ns

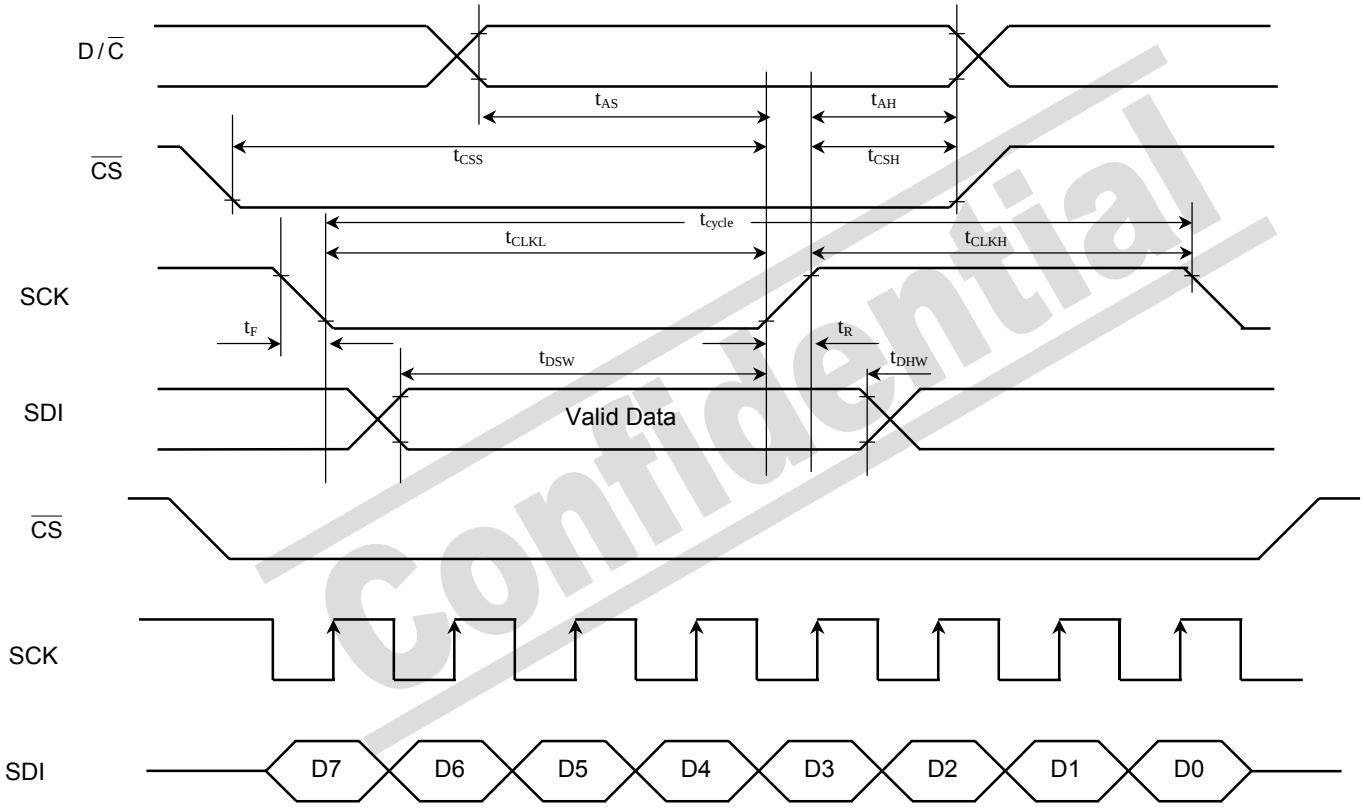


Figure 10 - 4 wire Serial Timing Characteristics

15 ITO resistance requirement

Pin Group	Pin Names	Suggested Maximum resistance
Primary booster	VCI, VCIX2, VCHS	10 Ω
Secondary booster	C1N, C1P, C2N, C2P, C3N, C3P, VGH, VGOFFL	20 Ω
Ground	VSS, AVSS, VSSRC	10 Ω
Power supply	VDD, VDDEXT	20 Ω
Current saving	CDUM0, CDUM1	20 Ω
Others	VCIM	20 Ω

16 GDDRAM Address

	RL=1	S0	S1	S2	S3	S4	S5	S6	S7	S8	…	S390	S391	S392	S393	S394	S395	
	RL=0	S395	S394	S393	S392	S391	S390	S389	S388	S387	…	S5	S4	S3	S2	S1	S0	
	BGR=0	R	G	B	R	G	B	R	G	B	…	R	G	B	R	G	B	Vertical address
	BGR=1	B	G	R	B	G	R	B	G	R	…	B	G	R	B	G	R	
TB=1	TB=0																	
G0	G131	0000H			0001H			0002H			…	0082H			0083H			0
G1	G130	0100H			0101H			0102H			…	0182H			0183H			1
G2	G129	0200H			0201H			0202H			…	0282H			0283H			2
G3	G128	0300H			0301H			0302H			…	0382H			0383H			3
G4	G127	0400H			0401H			0402H			…	0482H			0483H			4
.	.	.			.			.			.	.			.			.
.	.	.			.			.			.	.			.			.
.	.	.			.			.			.	.			.			.
G128	G3	8000H			8001H			8002H			…	8082H			8083H			128
G129	G2	8100H			8101H			8102H			…	8182H			8183H			129
G130	G1	8200H			8201H			8202H			…	8282H			8283H			130
G131	G0	8300H			8301H			8302H			…	8382H			8383H			131

Horizontal address	0	1	2	…	130	131

Remark : The address is in yyxxH format, where yy is the vertical address and xx is the horizontal address

17 Interface Mapping

1) Mapping for Writing an Instruction

		Hardware pins																	
Interface	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x
16 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8		IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
9 bits	1st										IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x
	2nd										IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x
8 bits	1st										IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	
	2nd										IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	

Remark : x Don't care bits

Not connected pins

2) Mapping for Writing Pixel Data(s)

16 bits	**262k**	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	
	65k		R4	R3	R2	R1	R0	G5	G4	G3		G2	G1	G0	B4	B3	B2	B1	B0	
9 bits	262k	1st										R5	R4	R3	R2	R1	R0	G5	G4	G3
		2nd										G2	G1	G0	B5	B4	B3	B2	B1	B0
8 bits	**262k**	1st										R5	R4	R3	R2	R1	R0	x	x	
		2nd										G5	G4	G3	G2	G1	G0	x	x	
		3rd										B5	B4	B3	B2	B1	B0	x	x	
	65k	1st										R4	R3	R2	R1	R0	G5	G4	G3	
		2nd										G2	G1	G0	B4	B3	B2	B1	B0	

Remark : x Don't care bits

Not connected pins

18 SSD1283A OUTPUT VOLTAGE RELATIONSHIP

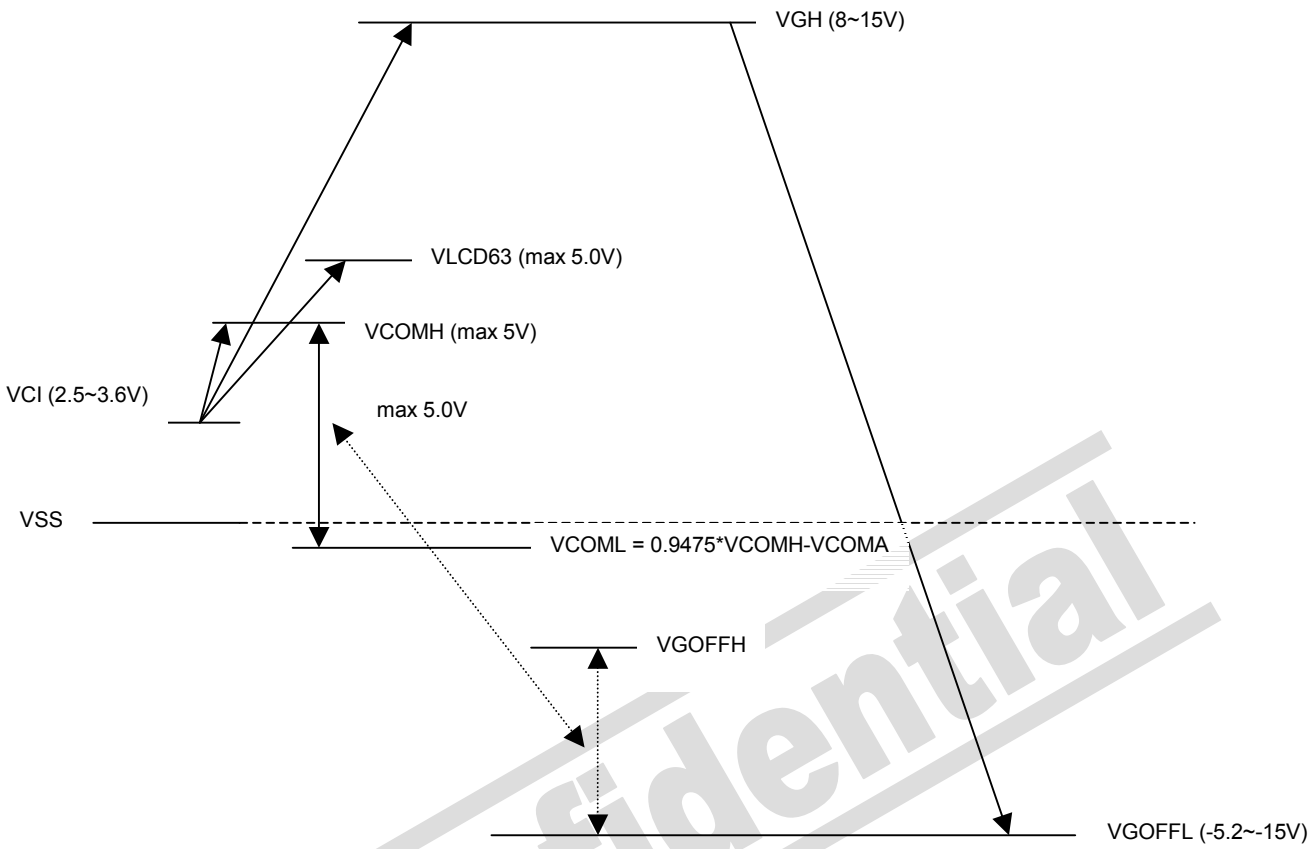


Figure 11 - LCD Driving Voltage Relationship

19 APPLICATION CIRCUIT

Figure 12 - Booster Capacitors

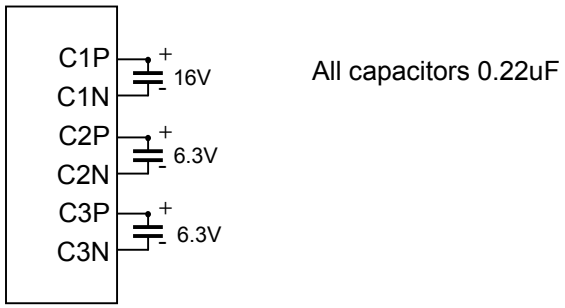


Figure 13 - Filtering and Charge Sharing Capacitors

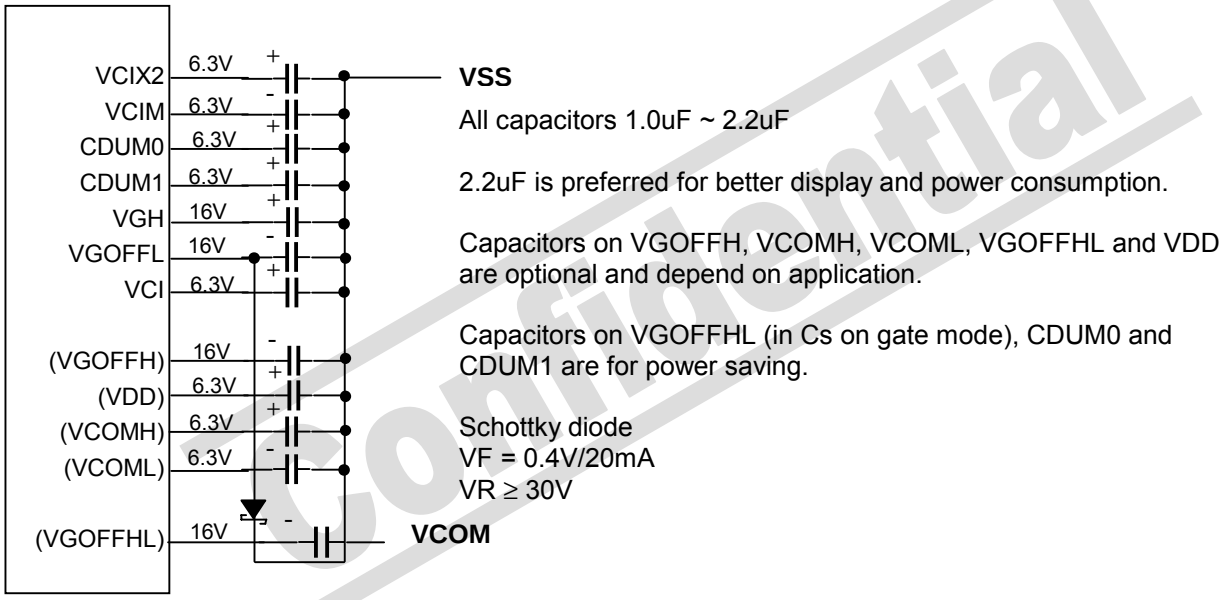
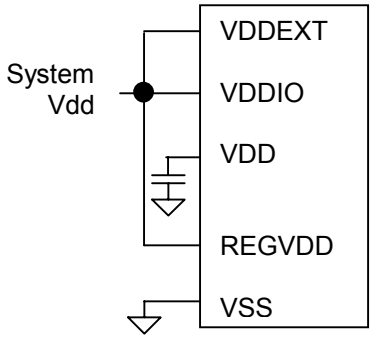
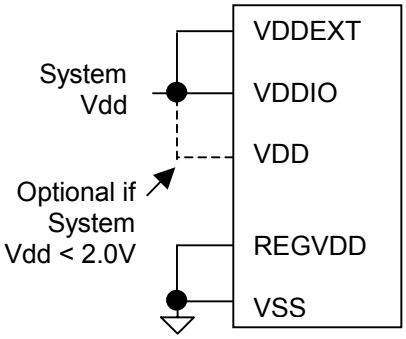


Figure 14 - Power Supply Pins Connections

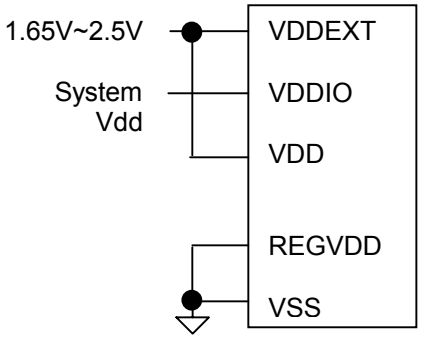
3.6V ≥ System Vdd > 2.5V



2.5V ≥ System Vdd > 1.65V
(REGVDD can be connected to either VDDIO or VSS)



1.65V ≥ System Vdd > 1.16V



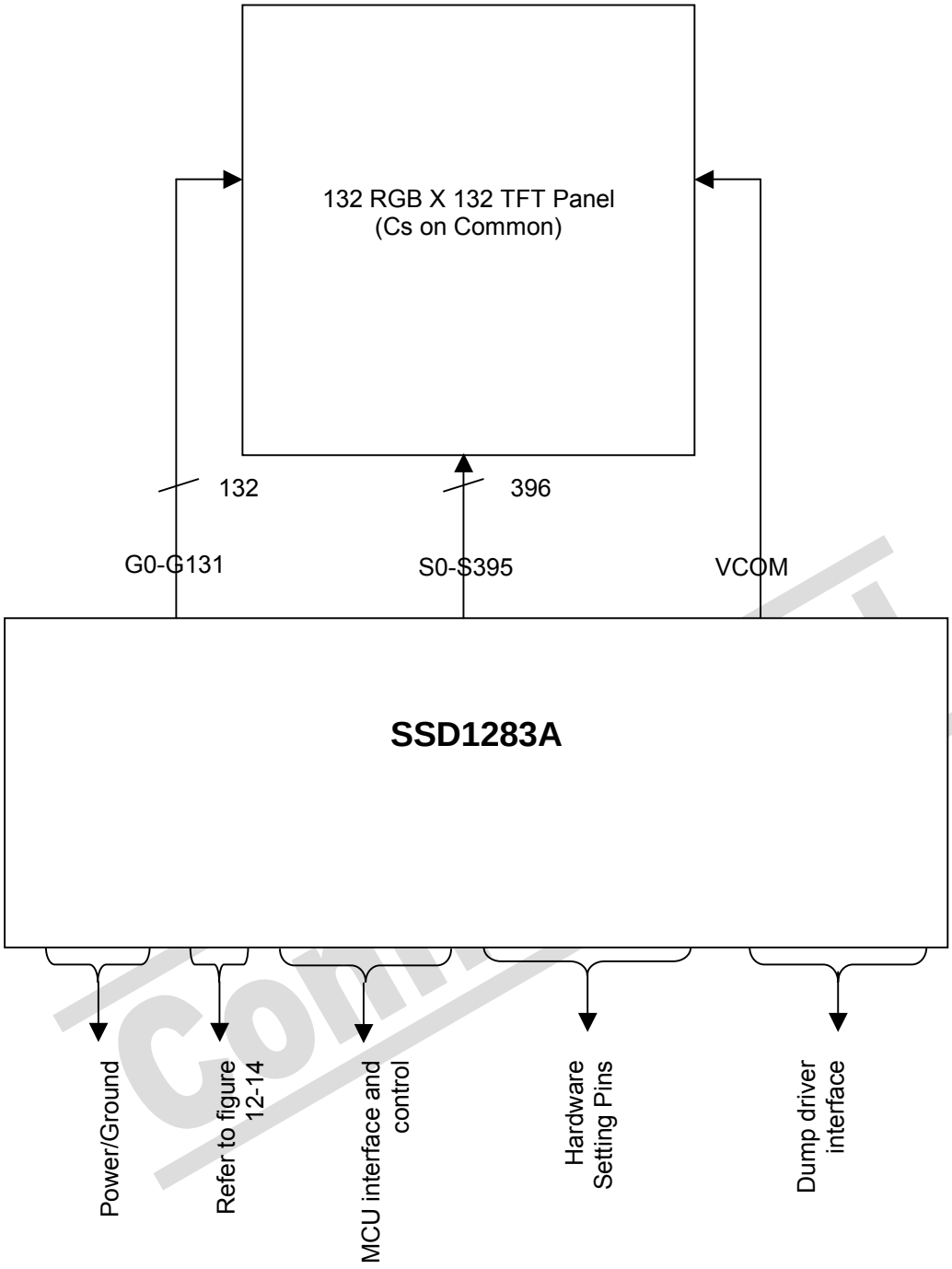
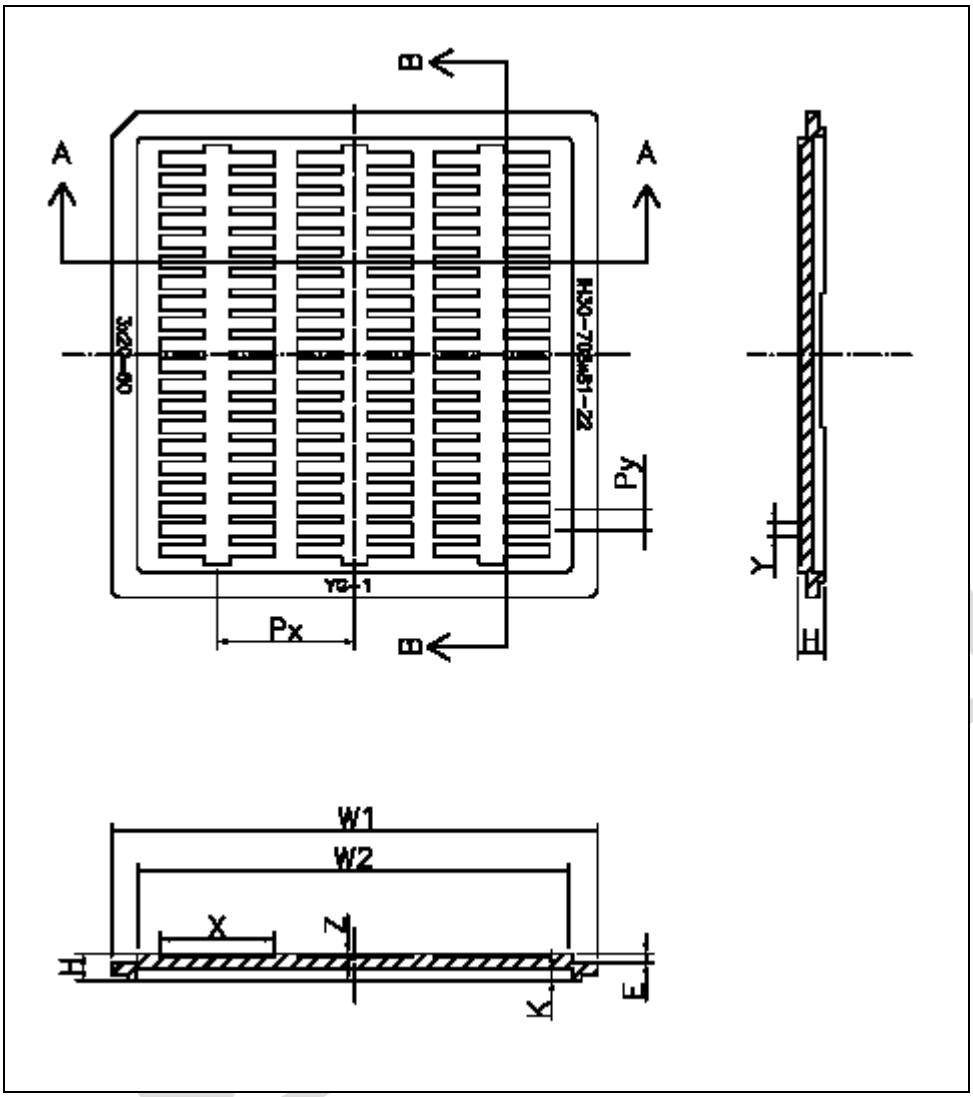


Figure 15 - Panel Connection Example (with external resistor for panel trimming)

20 Package Information

20.1 Die Tray Dimension



	Spec	
	mm	(mil)
W1	76.0 ± 0.2	(2992)
W2	68.0 ± 0.2	(2677)
H	4.20 ± 0.1	(165)
E	1.60 ± 0.1	(63)
K	1.50 ± 0.1	(59)
Px	21.49 ± 0.1	(646)
Py	3.22 ± 0.1	(127)
X	17.99 + 0.1	(708)
Y	2.05 + 0.1	(81)
Z	0.56 ± 0.05	(22)
N	60	

21 OTP Detail

Fresh die

1) **Example 1 - VCMR[5:0] is as default**

A fresh SSD1283A will have the OTP register default value of OTPR[5:0]=0x00 and R1F default value of VCMR[5:0]=0x36, which corresponds to base values [110110] from the 6 least significant bits.

VCMR[5:0]	1	1	0	1	1	0
OTPR[5:0]	0	0	0	0	0	0
VCOMH = VCMR XOR OTPR	1	1	0	1	1	0

2) **Example 2 - VCMR[5:0] is adjusted**

VCMR[5:0] will exclusive or (XOR) with the OTPR default value (0x00) to form a new VCOMH default value, and it is recommended to set this command right after the power control commands when applicable.

For example, when VCMR[5:0]=0x0030 which corresponding to [110000], the resultant VCOMH will be as below.

VCMR[5:0]	1	1	0	0	0	0
OTPR[5:0]	0	0	0	0	0	0
VCOMH = VCMR xor OTPR	1	1	0	0	0	0

The new VCOMH default value will become, 0x30

(Please be noted that preceding 10'b is added to the result so as to have uniformity as R1E command is sent.)

3) **Example 3 - VCM[5:0] is adjusted and nOTP=1**

nOTP=1 will override the default VCOMH value and is used together with VCM[5:0] to find out the optimal value against flickering.

Purpose VCMR[5:0] and OTPR[5:0] is the same as example 2.

For example, when nOTP=1 and VCM[5:0]=0x36 which corresponding to [110110], the resultant VCOMH will equal VCM regardless the value of VCMR XOR OTPR.

VCM[5:0]	1	1	0	1	1	0
VCOMH = VCM	1	1	0	1	1	0

The new VCOMH value will become, 0x36

(Please be noted that preceding 10'b is added to the result so as to have uniformity as R1E command is sent.)

Program OTP

When nOTP=1, R1E command is mainly used to find out the optimal value against flickering. The OTPR will be programmed as below.

(The equivalent VCOMH value is simply VCM[5:0] if nOTP is 1)

1) Example 1 - VCMR[5:0] is as default, target VCOMH value is equivalent to VCM[5:0] = 0x30.

When R1E-0x00B0 is sent, VCM[5:0] will be [110000]. The OTPR will be the XOR result of VCM[5:0] and VCMR[5:0]. In this case, VCMR[5:0] is the default = 0x36.

VCM[5:0]	1	1	0	0	0	0
VCMR[5:0]	1	1	0	1	1	0
OTPR[5:0]	0	0	0	**1**	**1**	0

The result in OTPR means bit 2 and bit 1 in OTPR[5:0] are programmed.

Example 2 – VCMR[5:0]=0x30 is adjusted, target VCOMH value is equivalent to VCM[5:0] = 0x30.

For optimum performance against flickering with different panel characteristic, VCMR[5:0] can be adjusted to reduce the frequency on OTP execution.

For VCMR[5:0]=0x30 is adjusted, and VCOMH target is same as VCM[5:0]=0x30, the below result shows that OTP is not required if VCMR[5:0] is adjusted.

VCM[5:0]	1	1	0	0	0	0
VCMR[5:0]	1	1	0	0	0	0
Result OTPR[5:0]	**0**	**0**	**0**	**0**	**0**	**0**

However, SSD1283A requires VCMR[5:0]=0x30 to be updated when power up every time in order to produce the target VCOMH value of VCM[5:0]=0x30

VCMR[5:0]	1	1	0	0	0	0
OTPR	0	0	0	0	0	0
VCOMH = VCMR xor OTPR	1	1	0	0	0	0

Please be reminded that OTP registers can be fired once and cannot be recovered, it is recommended to finalize the optimal OTP value before firing.

Example 3 – VCMR[5:0]=0x30 is adjusted, target VCOMH value is equivalent to VCM[5:0] = 0x31.

Upon process variation, there may be a variation in the panel characteristic, OTP may be used to adapt this.

VCMR[5:0] is adjusted to 0x30 as example 2 to reduce the frequency on OTP execution.

For VCM[5:0]=0x31 is adjusted to adapt the process variation, and VCOMH target is same as VCM[5:0]=0x31, the below result shows that only bit 1 of OTPR is required for programming if VCMR[5:0] is adjusted.

VCM [5:0]	1	1	0	0	0	1
VCMR[5:0]	1	1	0	0	0	0
Result OTPR	**0**	**0**	**0**	**0**	**0**	**1**

However, SSD1283A requires VCMR[5:0]=0x30 to be updated when power up every time in order to produce the target VCOMH value of VCM[5:0]=0x31

VCMR[5:0]	1	1	0	0	0	0
OTPR	0	0	0	0	0	1
VCOMH = VCMR XOR OTPR	**1**	**1**	**0**	**0**	**0**	**1**

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