

BoT-DAT100N

Specification

CONFIDENTIAL INFORMATION

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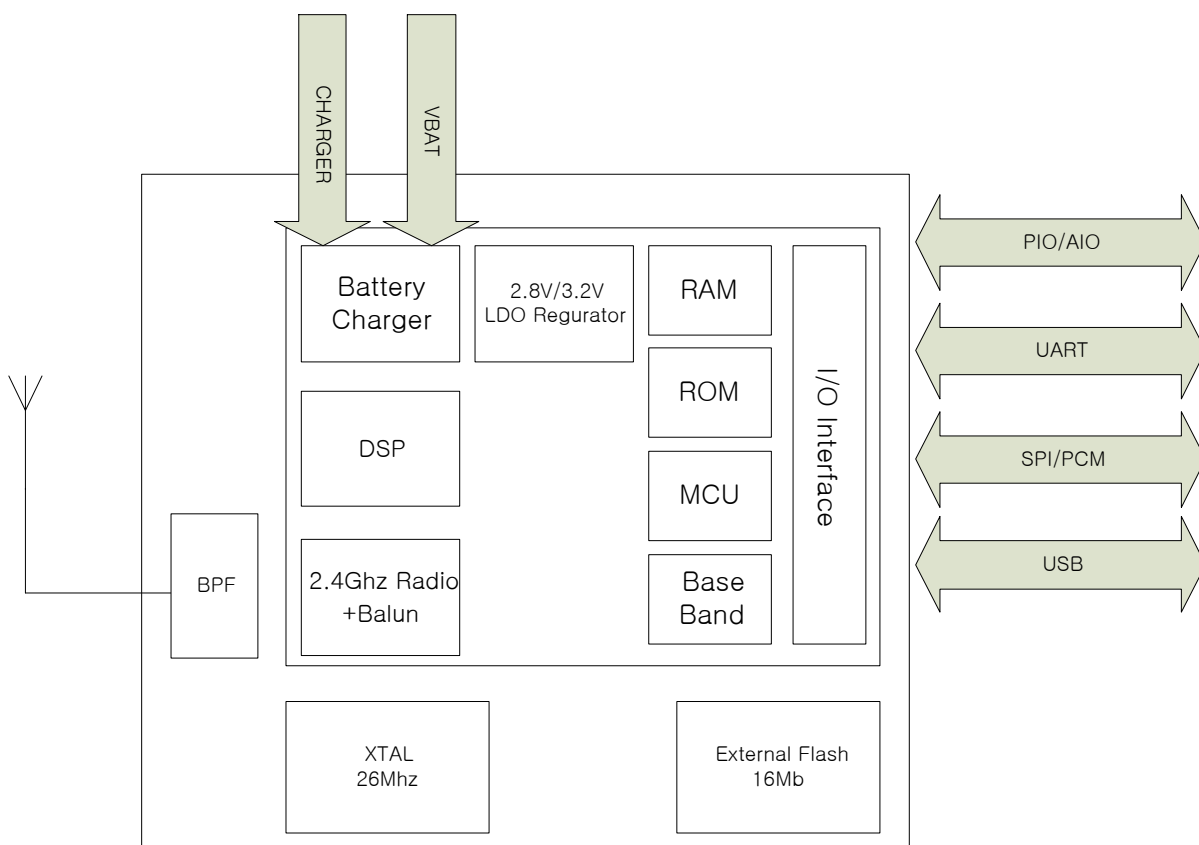
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1. General

1.1 Overview

This specification covers Bluetooth module which complies with Bluetooth specification version 4.1 and integrates RF & Baseband controller in small package. This Module has deployed CSR's CSRB5342 chipset.

All detailed specification including pin outs and electrical specification may be changed without notice.



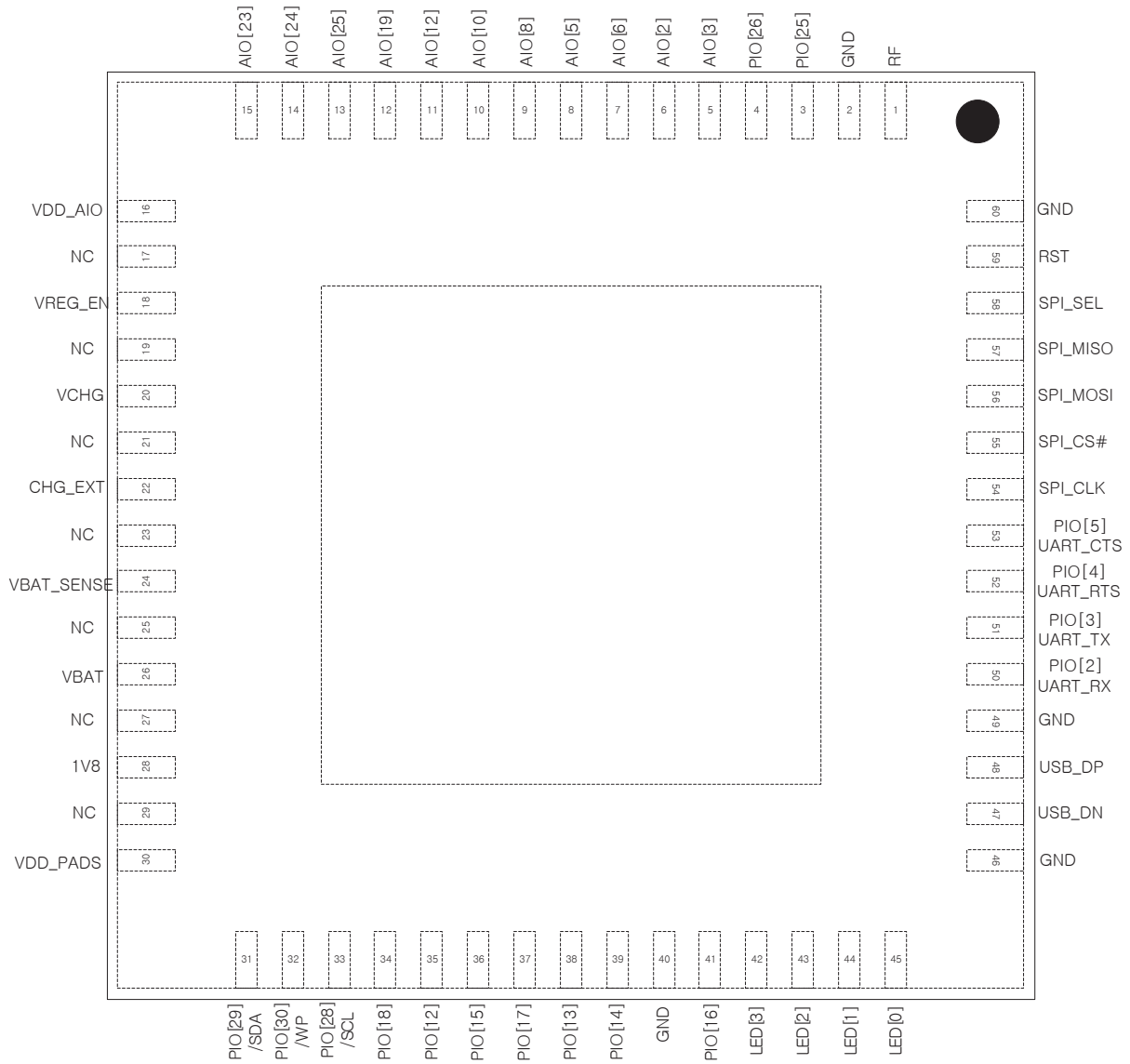
1.2 Features

- Bluetooth® v4.1 specification compliant
- Radio includes integrated balun and typical RF performance of 7 dBm transmit power and -88 dBm receive sensitivity ($\pi/4$ -DQPSK modulation)
- 80 MHz RISC MCU
- Programmable DSP with 4K x 32-bit program
- Serial interfaces: UART, USB 2.0 full-speed, I²C and SPI
- Up to 16 PIOs, i.e.9 general purpose PIOs and unused digital interfaces are available as PIOs
- Integrated battery charger
- Integrated to 16Mbit external Flash memory
- 4 on dedicated LED pads
- Power-on-reset detects low supply voltage
- Competitive Size
 - A type : 13mm x 13mm x 1.6mm : 60Pin
 - B type : 13mm x 13mm x 2.35mm : 60Pin (with SHIELD CAN.)
- Operating temperature range (MAX -20°C ~ 70°C)

1.3 Application

- Mobile Printer
- Wireless gaming Controllers
- Wireless HCI

1.4 Pin Configuration



Pin Configuration (TOP VIEW)

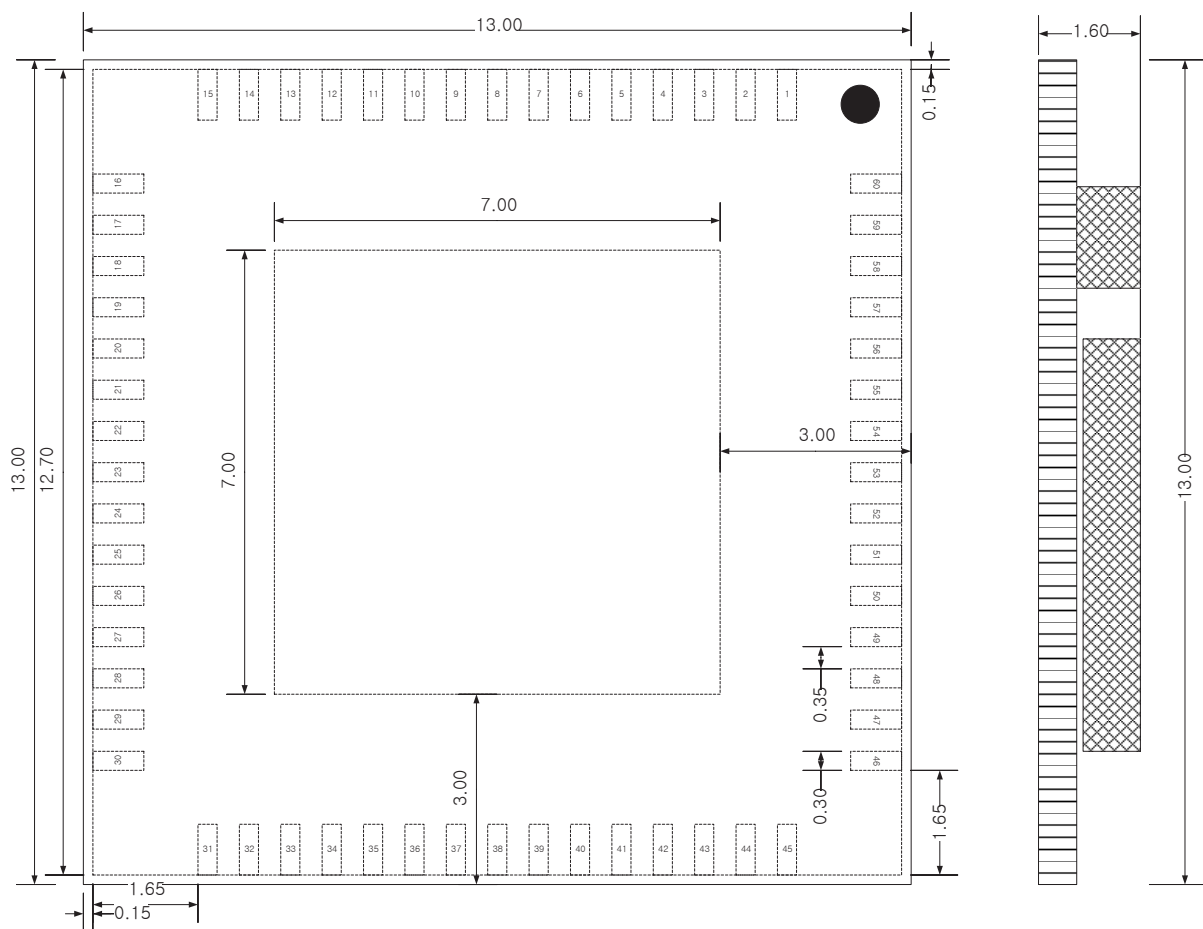
1.5 Device Terminal Functions

Function		Pin Name	Pin No.	Pin type	Description	Note
RF	RF	ANT	1	RF	Bluetooth 50Ω transmitter output / receiver input	
Function		Pin Name	Pin No.	Pin type	Description	Note
PIO	PIO [12]	PIO [12]	35	Bidirectional with weak pull-down	Programmable input/output line	
	PIO [13]	PIO [13]	38			
	PIO [14]	PIO [14]	39			
	PIO [15]	PIO [15]	36			
	PIO [16]	PIO [16]	41			
	PIO [17]	PIO [17]	37			
	PIO [18]	PIO [18]	34			
	PIO [25]	PIO [25]	3	Open-drain, bidirectional Hi-Z		
	PIO [26]	PIO [26]	4			
	AIO [2]	AIO [2]	6	Bidirectional Hi-Z	Analogue Programmable input/output line	
	AIO [3]	AIO [3]	5			
	AIO [6]	AIO [6]	7			
	AIO [5]	AIO [5]	8			
	AIO [8]	AIO [8]	9			
	AIO [10]	AIO [10]	10			
	AIO [12]	AIO [12]	11			
	AIO [19]	AIO [19]	12			
	AIO [23]	AIO [23]	15			
	AIO [24]	AIO [24]	14			
	AIO [25]	AIO [25]	13			

Function		Pin Name	Pin No.	Pin type	Description	Note
USB	USB_P	USB_P	48	Bidirectional	USB data plus with selectable internal 1.5kΩ pull-up resistor	
	USB_N	USB_N	47		USB data minus	
I2C	SDA	PIO[29]	SDA	Bidirectional weak pull-up	Programmable input/output line 29 Alternative function : I2C_SDA	
	SCL	PIO[28]	SCL		Programmable input/output line 28 Alternative function : I2C_SCL	
	WP	PIO[30]	WP		Programmable input/output line 30 Alternative function : I2C_WP	
SPI	SPI_MISO	PCM_OUT	SPI_MISO	57	Output with weak pull-down	SPI data output
	SPI_MOSI	PCM_IN	SPI_MOSI	56	Input with weak pull-down	SPI data input
	SPI_CS#	PCM_SYNC	SPI_CS#	55		Chip select for SPI, active low
	SPI_CLK	PCM_CLK	SPI_CLK	54		SPI clock
	SPI_SEL	PCM_SEL	SPI_SEL	58	Input with strong pull-down	SPI select
UART	UART_RX	PIO[2]	UART_RX	50	Bidirectional with weak pull-down	Programmable input/output line 2 Alternative function : UART_RX
	UART_TX	PIO[3]	UART_TX	51		Programmable input/output line 3 Alternative function : UART_TX
	UART_RTS	PIO[4]	UART_RTS	52		Programmable input/output line 4 Alternative function : UART_RTS
	UART_CTS	PIO[5]	UART_CTS	53		Programmable input/output line 5 Alternative function : UART_CTS
LED	LED [0]	LED [0]	45	Open drain	LED Driver	
	LED [1]	LED [1]	44		LED Driver	
	LED [2]	LED [2]	43		LED Driver	
	LED [3]	LED [3]	42		LED Driver	
Other Pin	VDD_AIO	VDD_AIO	16		Output of ADC regulator	
	VREGENABLE	VREG_EN	18	-	Regulator enable input	
	VCHG	VCHG	20	-	Battery charger input	
	CHG_EXT	CHG_EXT	22		External battery charger control	
	VBAT_SENSE	VBAT_SENSE	24	-	Battery charger sense input	
	VBAT	VBAT	26	-	Battery positive terminal	
	1V8	1V8	28	-	1V8 LDO regulator output	
	VDD_PADS	VDD_PADS	30		Positive supply for PIOs	
	RST#	RST#	59	Input with strong pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset.	
	GND	GND	2,40,46,49,60, EPAD		Ground	
NC	NC	17,19,21,23,25,27,29		Not connection		

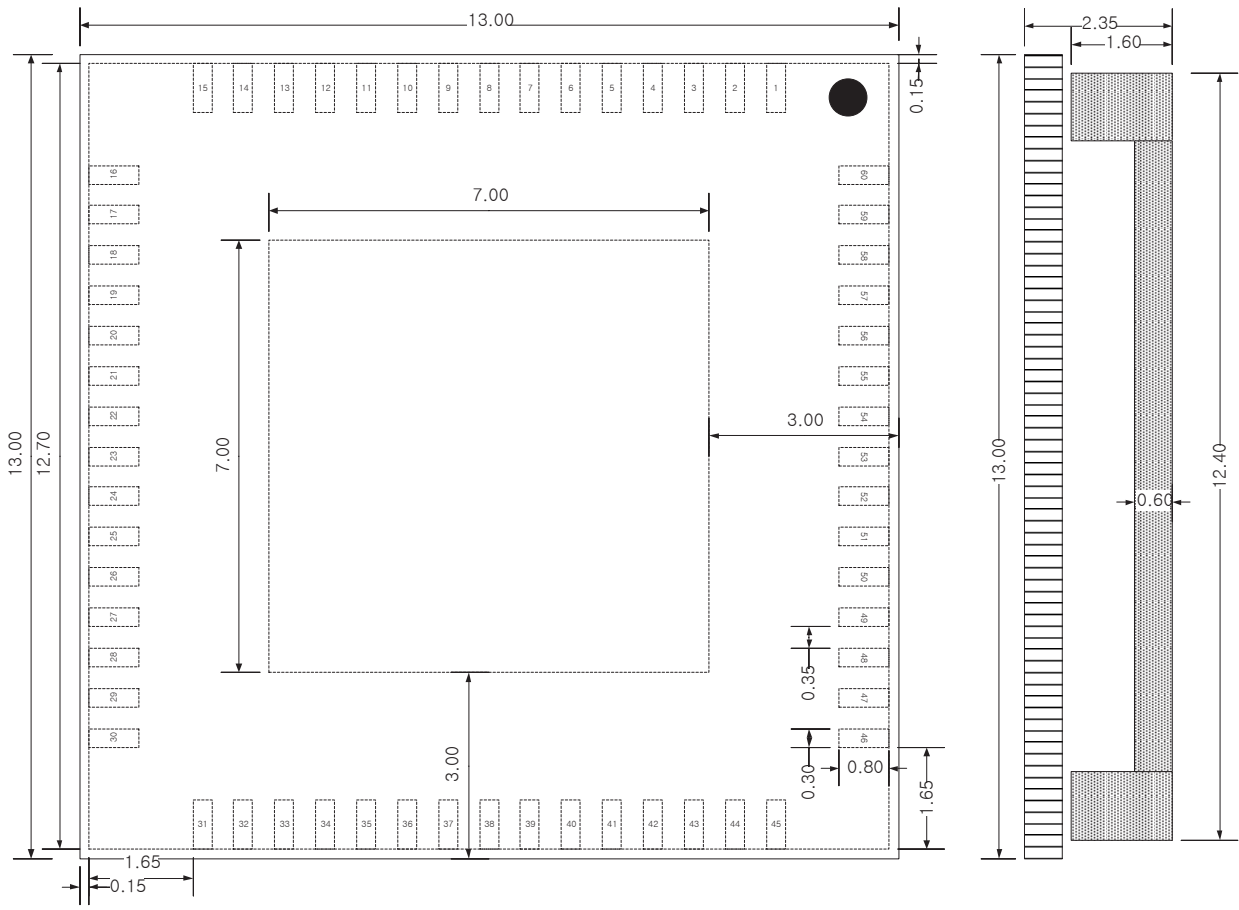
1.6 Package Dimensions & Land Pattern

- unit = mm
- General Tolerances = $\pm 0.2\text{mm}$



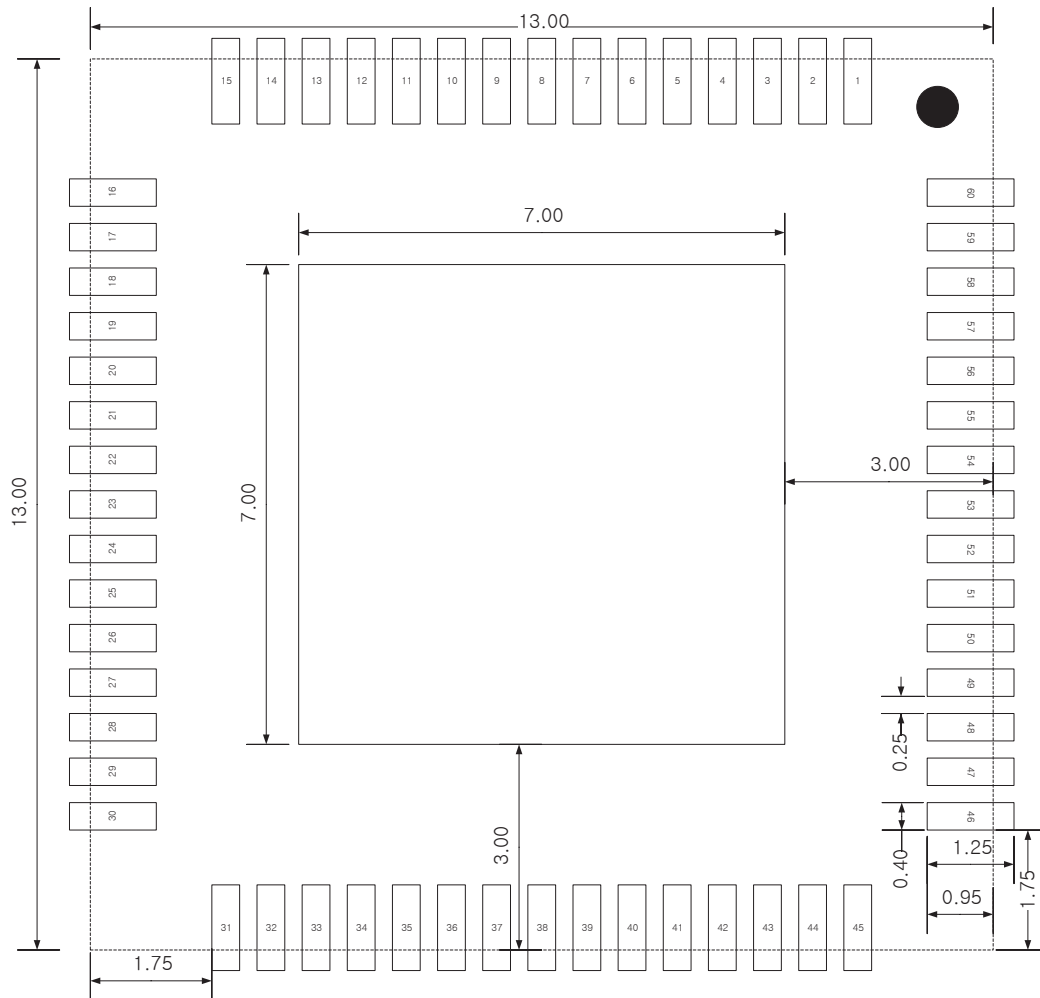
BoT-DAT100N A type Package Dimensions

- unit = mm
- General Tolerances = $\pm 0.2\text{mm}$



BoT-DAT100N B type Package Dimensions

● unit = mm



<Land Pattern>

2. Characteristics

2.1 Electrical Characteristics

■ Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage Temperature range		-40	85	°C
Charger	VCHG	-0.4	6.50	V
LEDs	LED[3:0]	-0.4	4.40	V
Battery	VBAT	-0.4	4.40	V
VDD_IO		-0.4	3.60	V
Other terminal voltages		VSS-0.4	VDD+0.4	V

■ Recommended Operating Conditions

Operating Condition		Min	TYP	Max	Unit
Operating Temperature range		-20	20	70	°C
Charger	VCHG	3.00	5.00	6.50	V
Battery	VBAT	2.70	3.70	4.30	V
LEDs	LED[3:0]	1.10	3.20	4.30	V
VDD_IO		1.70	1.8	3.60	V

■ 1.8V LDOOUT

Normal Operating		Min	TYP	Max	Unit
Output voltage		1.7	1.8	1.9	V
Load current		-	-	100	mA

■ ADC LDO OUT

Internal LDO		Min	TYP	Max	Unit
Output voltage		2.50	2.8/3.2	3.232	V
Load current		-	-	100	mA

■ Battery Charger

Battery Charger		Min	TYP	Max	Unit
Input voltage, VCHG		4.75	5	6.5	V
Trickle Charge		Min	TYP	Max	Unit
Charge current $I_{trickle}$, as percentage of fast charge current		8	10	12	%
V_{fast} rising threshold		-	2.9/3.0/3.1/3.2	-	V
V_{fast} rising threshold trim step size		-	0.1	-	V
V_{fast} falling threshold		-	2.8	-	V
$I_{trickle}$ in internal mode		1	-	20	mA
$I_{trickle}$ in internal mode step size			1		mA
Fast charge		Min	TYP	Max	Unit
Charge current during constant current mode, I_{fast}	Maximum charge setting (VCHG>VBAT+550mV)	194	200	206	mA
	Minimum charge setting (VCHG>VBAT+550mV)	-	10	-	mA
Reduced headroom charge current, as a percentage of I_{fast}	(VCHG=VBAT + 550mV)	50	-	100	%
Charge current step size		-	10	-	mA
V_{float} threshold, CSR calibrated to 4.2V		4.16	4.20	4.24	V
V_{float} threshold adjustment		3.58	4.20	4.42	V
V_{float} threshold adjustment step size		-	56	-	mV
V_{hyst} : Voltage VBAT needs to fall from V_{float} before charging restarts with 4.20 V V_{float} (selectable), 1%		-	3.77/3.86/3.94/4.08	-	V
Charge termination current I_{term} , as percentage of I_{fast}		7	10	20	%
Error		Min	TYP	Max	Unit
Headroom (VCHG- VBAT) falling threshold		-	50	-	mV
High Current Charging (External Mode)		Min	TYP	Max	Unit
Fast Charge current, I_{fast}		200	-	500	mA
Control current into CHG_EXT		0	-	20	mA
Voltage on CHG_EXT		0	-	6.50	V
External pass device H_e		25	50	270	-
Sense voltage, between VBAT_SENSE and VBAT at maximum current		195	200	205	mV
$I_{trickle}$ in external mode		12.5		50	mA
$I_{trickle}$ in external mode step size		-	2.5	-	mA

■ 12-bit ADC

12-bit ADC		Min	TYP	Max	Unit
Resolution(VDD_ADC =2.8V/3.2V)		-	-	12	Bits
Input voltage range		0	-	VDD_ADC	KHz
Accuracy (VDD_ADC=2.8V/3.2V Only)	INL			+/-1.5	LSB
(Guaranteed monotonic)	DNL			+/-1.5	LSB
Offset				+/-1.5	LSB
Gain error				+/-1.5	LSB
Conversion tim		14	14		μs
External source impedance				50	kΩ
Sample and hold capacitance			12		pF

■ Digital Terminals

Input Voltage Levels	Min	TYP	Max	Unit
V _{IL} input logic level low	-0.4	-	0.25xVDD	V
V _{IH} input logic level high	0.7 x VDD	-	VDD+0.4	V
T _r /T _f	-	-	25	ns
Output Voltage Levels	Min	TYP	Max	Unit
V _{OL} output logic level low, b _L = 4.0mA	-	-	0.4	V
V _{OH} output logic level high, φ _H = -4.0mA	0.75 x VDD	-	-	V
T _r /T _f	-	-	5	ns
Input and Tristate Currents	Min	TYP	Max	Unit
Strong pull-up	-150	-40	-10	μA
Strong pull-down	10	40	150	μA
Weak pull-up	-5	-1.0	-0.33	μA
Weak pull-down	0.33	1	5	μA
C _I Input Capacitance	1	-	5	pF
High impedance state (no pulls)	-0.1	0	0.1	μA

■ Open Drain PIO [25:26]

Input Voltage Levels	Min	TYP	Max	Unit
V _{IL} input logic level low	-0.4	-	0.4	V
V _{IH} input logic level high	1.0	-	4.3	V
T _r /T _f	-	-	25	ns
Current Sink Capability	Min	TYP	Max	Unit
Current IPAD, driving low	-	-	0.4	V
Current IPAD, high impedance	0.75x VDD	-	-	V
Optional pull-down	-	-	5	ns

■ AIO Terminals (when used as digital I/O)

Input Voltage Levels		Min	TYP	Max	Unit
V _{IL} input logic level low		-0.4	-	0.25x VDD_AIO	V
V _{IH} input logic level high		0.7 x VDD_AIO	-	VDD_AIO+ 0.4	V
T _r /T _f		-	-	25	ns
Output Voltage Levels		Min	TYP	Max	Unit
V _{OL} output logic level low, b _L = 8.0mA		-	-	0.4	V
V _{OH} output logic level high, φ _H = -4.0mA		0.75 x VDD_AIO	-	-	V
T _r /T _f		-	-	5	ns
Input and Tristate Currents		Min	TYP	Max	Unit
Weak pull-down		80	100	120	kΩ
C _I Input Capacitance		1	-	5.0	pF
High impedance state		-0.4	0	0.4	μA

■ LED Driver Pads

LED Driver Pads		Min	TYP	Max	Unit
Current, IPAD	High impedance state	-	-	5	μA
	Current sink state	-	-	50	mA
LED pad resistance Note : VDD_PADS1=3.2V	V _{PAD} < 0.5V	2.4	2.8	4.4	Ω

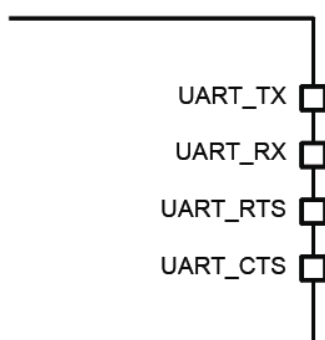
2.2 RF Characteristics

T.B.D

3. Terminal Description

3.1 UART Interface

This is a standard UART interface for communicating with other serial devices. BoT-DAT100N UART interface provides a simple mechanism for communicating with other serial devices using the RS-232 protocol.



When BoT-DAT100N is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement optional RS232 hardware flow control where both are active low indicators

If UART_CTS and UART_RTS are not required for hardware flow control, they are reconfigurable as PIO. UART configuration parameters, such as baud rate and packet format, are set using BoT-DAT100N firmware.

3.1.1 UART Setting

Parameter		Possible values
Baud rate	Minimum	1200 baud($\leq 2\%$ Error)
	Maximum	9600 baud($\leq 1\%$ Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

3.2 SPI Interface

BoT-DAT100N provides a debug SPI interface for programming, configuring and debugging the BoT-DAT100N. Access to this interface is required in production. Ensure the 4 SPI signals externally.

3.3 USB Interface

BoT-DAT100N has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices.
The USB interface on BoT-DAT100N acts as a USB peripheral, responding to requests from a master host controller.

3.4 I2C Interface

BoT-DAT100N supports a firmware controlled I²C interface to communicate with external EEPROM to store the PS Keys.
The I²C timing is compliant with the Philips I²C Specification (100 kHz and 400 kHz).

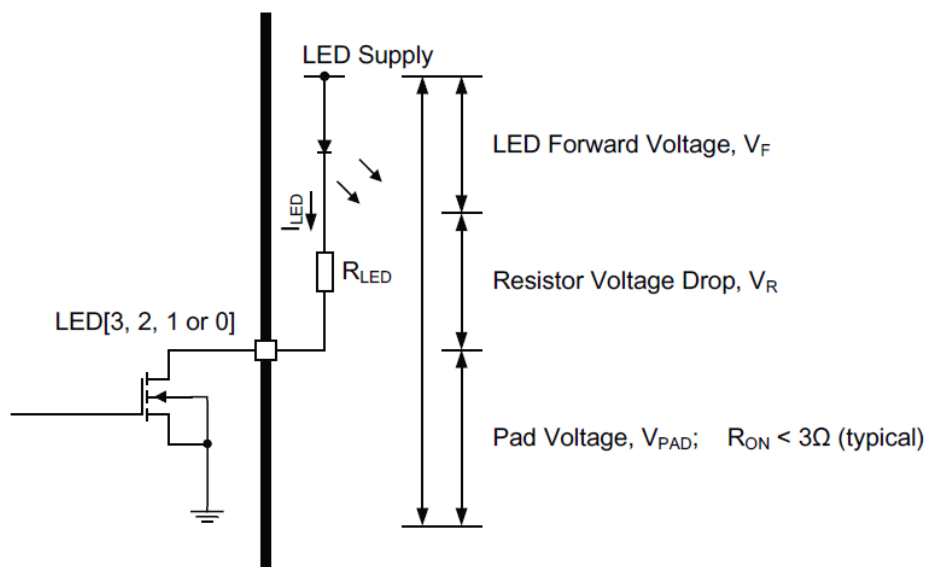
If an SPI flash device is used it is not necessary to use an EEPROM as PS Keys can be stored in the SPI flash.

EEPROM can only be used for PS Key storage and not VM applications.

3.5 LED Drivers

BoT-DAT100N includes a 4-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colors. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.



It is possible to derive below Equation to calculate I_{LED} . If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} is calculated.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

For the LED pads to act as resistance, the external series resistor, R_{LED} , needs to be such that the voltage drop across it, V_R , keeps V_{PAD} below 0.5V. Below equation also applies.

$$VDD = V_F + V_R + V_{PAD}$$

4. Battery Charger

4.1. Battery Charger Hardware Operating Modes

The battery charger hardware is controlled by the VM, see Section The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current, see the below Table and Figure.

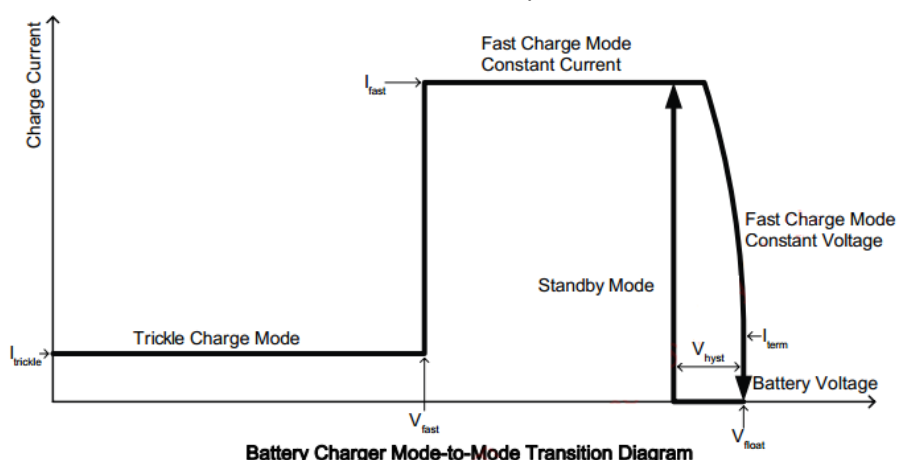
The internal charger circuit can provide up to 200mA of charge current, for currents higher than this the BoT-DAT100N can control an external pass transistor.

Mode	Battery Charger Enabled	VBAT_SENSE
Disabled	No	X
Trickle charge	Yes	>0 and $<V_{fast}$
Fast charge	Yes	$>V_{fast}$ and $<V_{float}$
Standby	Yes	$I_{term}^{(a)}$ and $>(V_{float} - V_{hyst})$
Error	Yes	$>(V_{CHG} - 50mV)$

Battery Charger Operating Modes Determined by Battery Voltage and Current

^(a) I_{term} is approximately 10% of I_{fast} for a given I_{fast} setting

Below figure shows the mode-to-mode transition voltages. These voltages are fixed and calibrated by CSR. The transition between modes can occur at any time.



Note:

The battery voltage remains constant in Fast Charge Constant Voltage Mode, the curved line on Figure is for clarity only.

5.1.1 Disable Mode

In the disabled mode the battery charger is fully disabled and draws no active current on any of its terminals.

5.1.2 Trickle Charge Mode

In the trickle charge mode, when the voltage on VBAT_SENSE is lower than the V_{fast} threshold, a current of approximately 10% of the fast charge current, I_{fast} , is sourced from the VBAT pin.

The V_{fast} threshold detection has hysteresis to prevent the charger from oscillating between modes.

5.1.3 Fast Charge Mode

When the voltage on VBAT_SENSE is greater than V_{fast} , the current sourced from the VBAT pin increases to I_{fast} .

I_{fast} is between 10 mA and 200 mA set by PS Key or a VM trap. In addition, I_{fast} is calibrated in production test to correct for process variation in the charger circuit.

The current is held constant at I_{fast} until the voltage at VBAT_SENSE reaches V_{float} , then the charger reduces the current

sourced to maintain a constant voltage on the VBAT_SENSE pin.

When the current sourced is below the termination current, I_{term} , the charging stops and the charger enters standby

mode. I_{term} is typically 10% of the fast charge current.

If External mode is selected, the charger controls the external transistor to provide the charge current

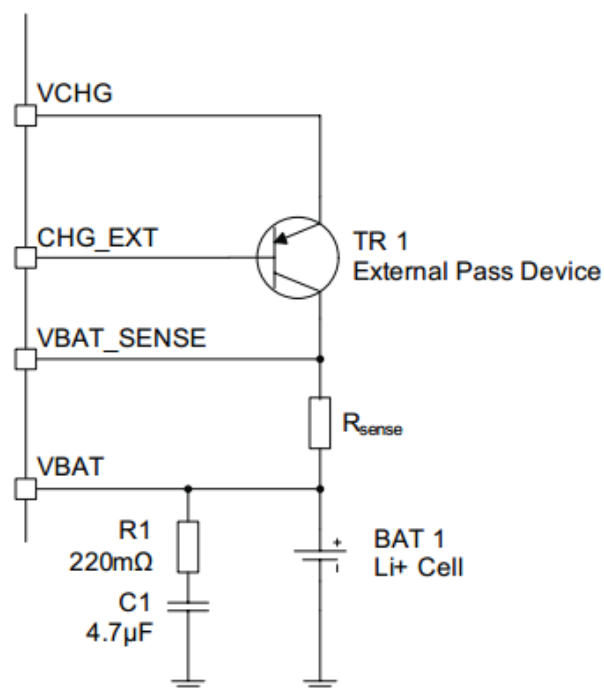
5.1.4 Standby Mode

When the battery is fully charged, the charger enters standby mode, and battery charging stops. The battery voltage on the VBAT_SENSE pin is monitored, and when it drops below a threshold set at V_{hyst} below the final charging voltage, V_{float} , the charger re-enters fast charge mode.

4.2 External Mode

The external mode is for charging higher capacity batteries using an external pass device. The current is controlled by sinking a varying current into the CHG_EXT pin, and the current is determined by measuring the voltage drop across a resistor, R_{sense} , connected in series with the external pass device. The voltage drop is determined by looking at the difference between the VBAT_SENSE and VBAT pins. The voltage drop across R_{sense} is typically 200mV. The value of the external series resistor determines the charger current. This current can be trimmed with a PS Key.

Below Figure R1 (220m Ω) and C1 (4.7 μ F) form an RC snubber that is required to maintain stability across all battery ESRs. The battery ESR must be <1.0 Ω .



Battery Charger External Mode Typical Configuration

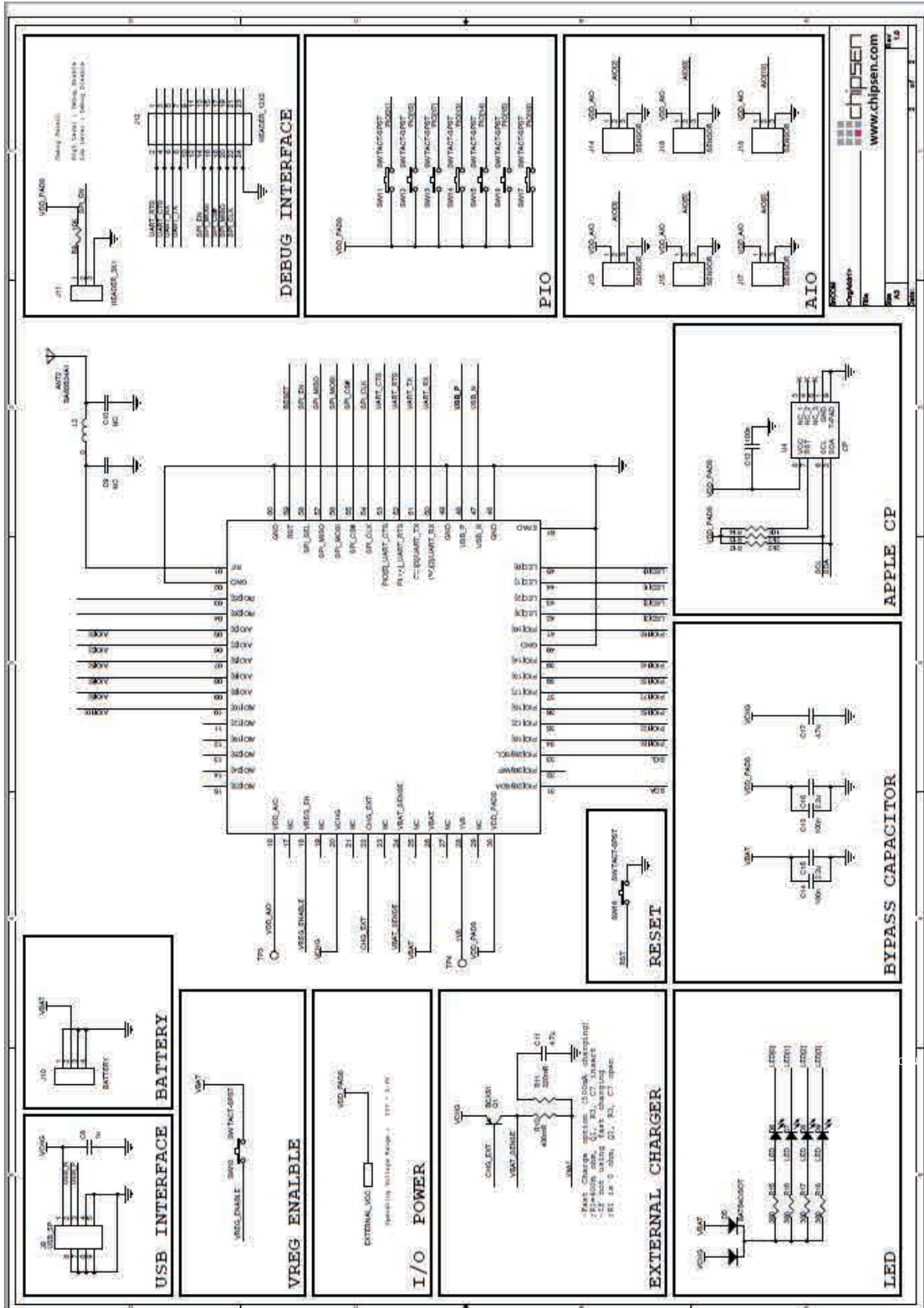
5. Reset, RST#

BoT-DAT100N is reset from several sources:

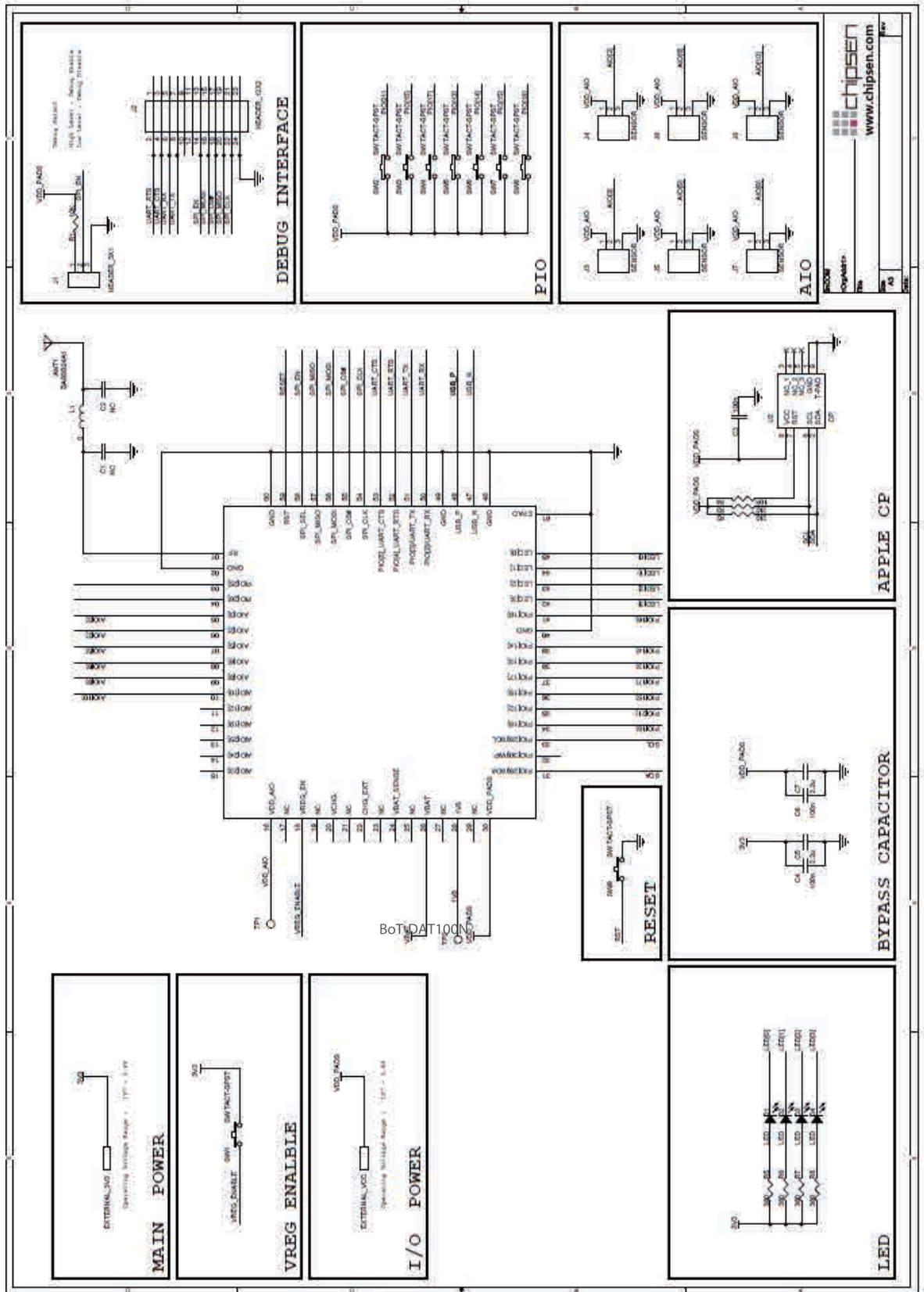
- RST# pin
- Power-on reset
- USB charger attach reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. CSR recommends applying RST# for a period >5ms.

6. Example- Battery Application Schematic



7. Example - 3V3 Supply Application Schematic



WARNING: For BoT-DAT100N

If you have reflow process multiple times in your product, you must be proceed this module in the final reflow process. If not the Shield can will drop out.