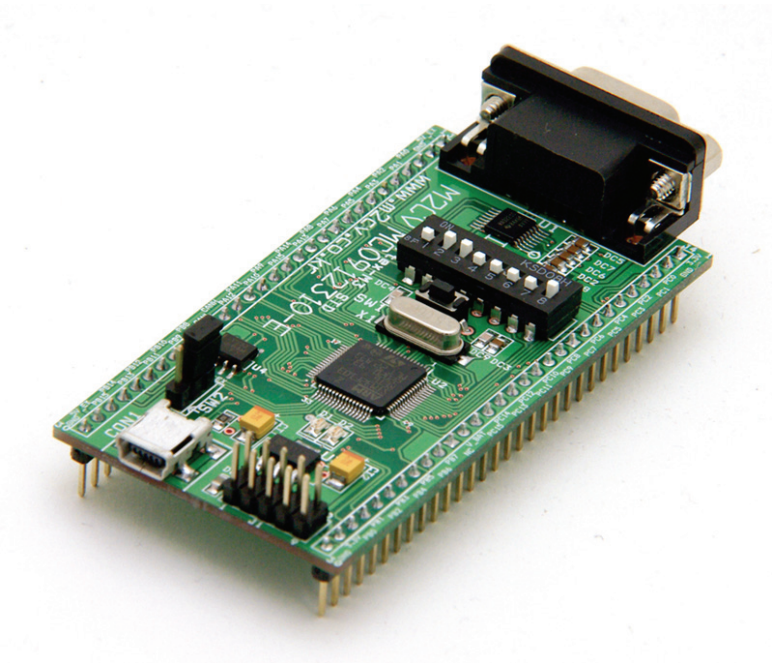
Cortex-M3



Cortex-M3(STM32F103) Standard v3.0 Manual

Machine Vision & Motion Control M2CV

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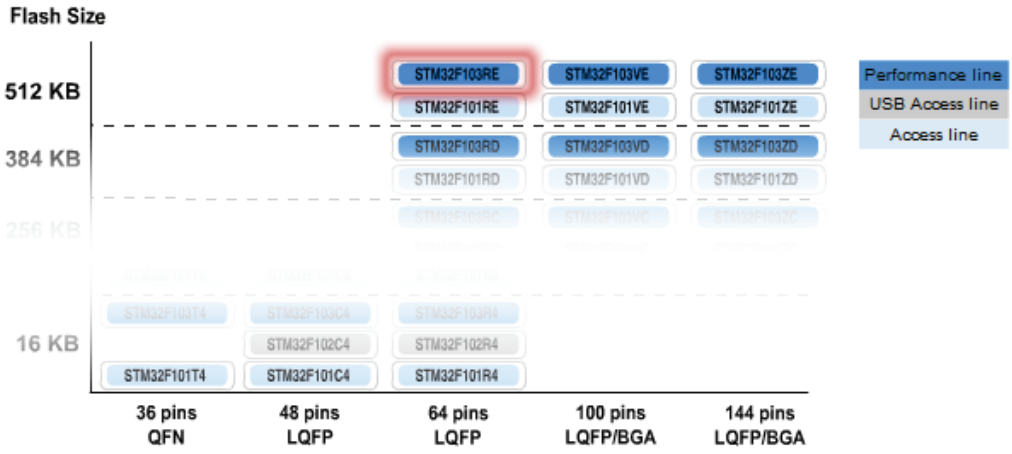
1. Features

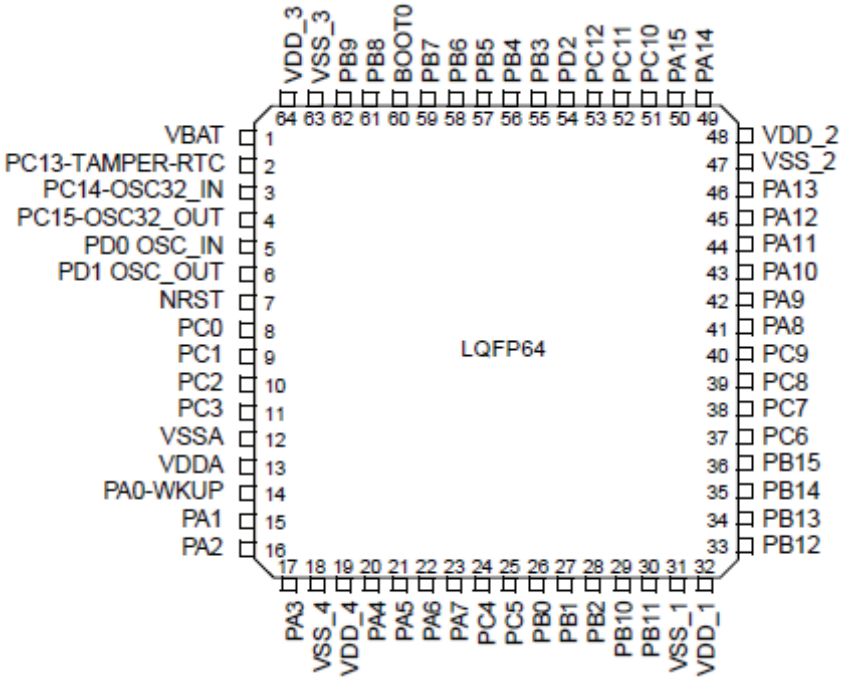
- ST사의 STM32F103RET6(시리즈 최상위) 채용
  - Core: ARM 32-bit Cortex™™-M3 CPU(72MHz, 1.25 DMIPS/MHz)
  - 512Kbytes of Flash memory, 64 Kbyte of SRAM
  - Clock, reset and supply management
  - Low power
  - 3 × 12-bit, 1 µs A/D converters (up to 21channels)
  - 2 × 12-bit D/A converters
  - DMA: 12-channel DMA controller
  - Debug mode
  - Up to 112 fast I/O ports
  - Up to 11 timers
  - Up to 13 communication interfaces
  - CRC calculation unit, 96-bit unique ID
- CAN Transceivers 채용
- 1열 디자인으로 브레드보드에 바로 사용
- 통신용 RS232 포트채용(Flash Downloading시에도 사용)
- USB 5V, 외장 전원 택일가능(3.3V 레귤레이터 내장)
- 1 x Power LED, 1 x User LED, 1 x Reset S/W
- 딥 스위치채용으로 기능사용및 변경 편리
- 10핀 J-Tag
- 42 x 78.5 x 2.54(Width x Height x Pin Pitch)



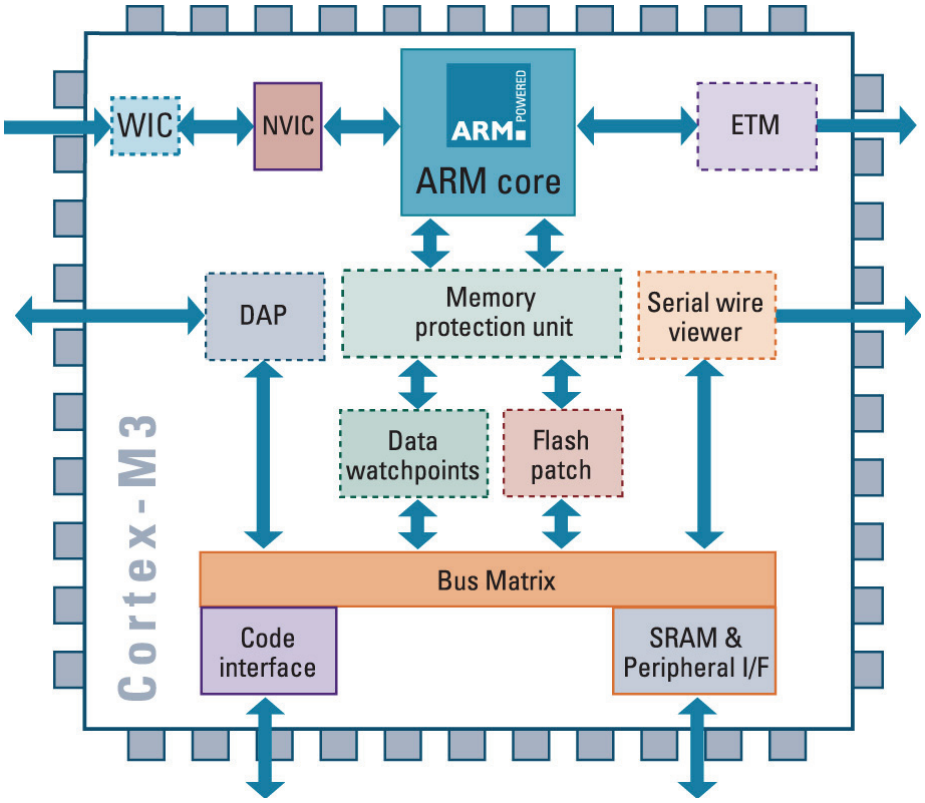
2. Applications

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

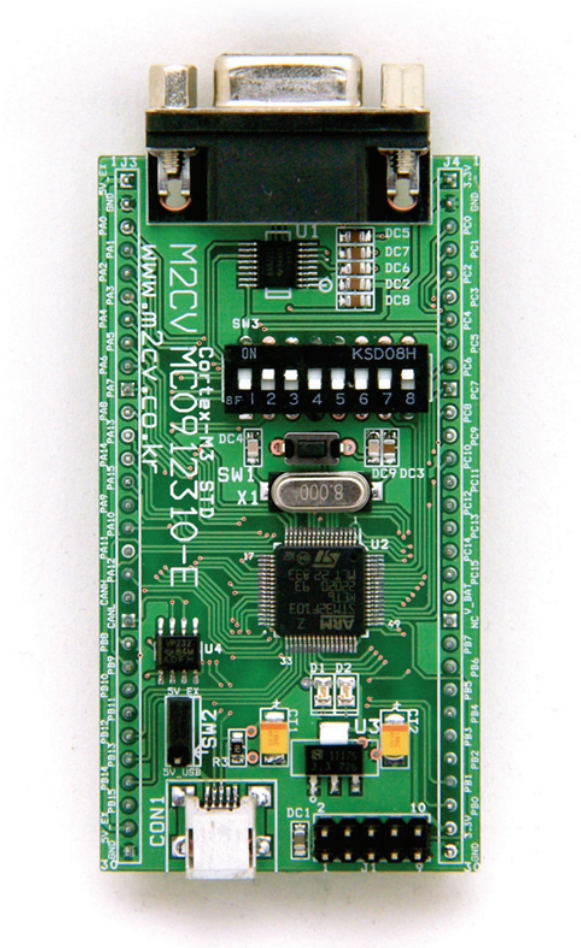
3. STM32F103RBT6 Pinout



4. STM32F Block Diagram



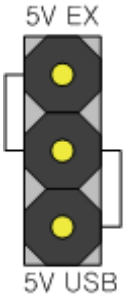
5. Board 구성



SW3

SW3 Funtion Table

1	Boot Select(ON:Downloading)
2	UART TXD
3	UART RXD
4	USB Data -
5	USB Data +
6	CAN RX
7	CAN TX
8	CAN Terminating Resistance

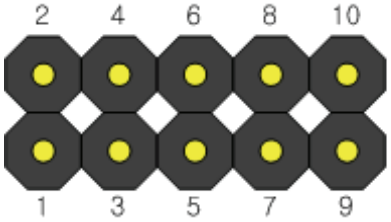


SW2

전원 선택 점퍼

- 5V EX : 외장 5V 연결시(J3 Pin1, Pin29 5V / Pin2, Pin30 GND)
- 5V USB : USB 전원 사용시

* 참고 : 5V USB 사용시 J3 Pin1, Pin29 / Pin 2, Pin30으로 5V가 출력되지 않습니다



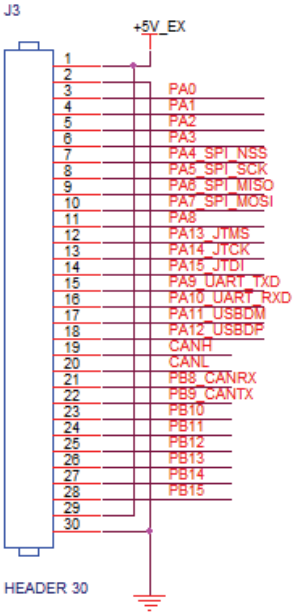
J1

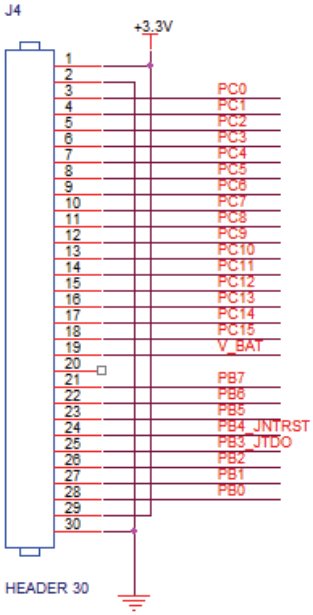
TMS	TCK	TDO	TDI	JNT RST
3.3V	GND	GND	NC	GND

6. M2CV Cortex-M3 Pins Assignment

Pin Header J3	
PIN 1	+5V
PIN 2	GND
PIN 3	PA0
PIN 4	PA1
PIN 5	PA2
PIN 6	PA3
PIN 7	PA4_SPI_NSS
PIN 8	PA5_SPI_SCK
PIN 9	PA6_SPI_MISO
PIN 10	PA7_SPI_MOSI
PIN 11	PA8
PIN 12	PA13_JTMS
PIN 13	PA14_JTCK
PIN 14	PA15_JTDI
PIN 15	PA9_UART_TXD
PIN 16	PA10_UART_RXD
PIN 17	PA11_USB_DM
PIN 18	PA12_USB_DP
PIN 19	CANH
PIN 20	CANL
PIN 21	PB8_CANRX
PIN 22	PB9_CANTX
PIN 23	PB10
PIN 24	PB11
PIN 25	PB12
PIN 26	PB13
PIN 27	PB14
PIN 28	PB15
PIN 29	+5V
PIN 30	GND

Pin Header J4	
PIN 1	+3.3V
PIN 2	GND
PIN 3	PC0
PIN 4	PC1
PIN 5	PC2
PIN 6	PC3
PIN 7	PC4
PIN 8	PC5
PIN 9	PC6
PIN 10	PC7
PIN 11	PC8
PIN 12	PC9
PIN 13	PC10
PIN 14	PC11
PIN 15	PC12
PIN 16	PC13
PIN 17	PC14
PIN 18	PC15
PIN 19	V_BAT
PIN 20	NC
PIN 21	PB7
PIN 22	PB6
PIN 23	PB5
PIN 24	PB4_JNTRST
PIN 25	PB3_JTDO
PIN 26	PB2
PIN 27	PB1
PIN 28	PB0
PIN 29	+3.3V
PIN 30	GND





6-1. STM32F Pin definitions Main Function & Alternate Functions

Pins	Pin Name	Main-Function	Alternate Functions	
			Default	Remap
1	V_{BAT}	V_{BAT}		
2	PC13-TAMPERRTC(4)	PC13(5)	TAMPER-RTC	
3	PC14-OSC32_IN(4)	PC14(5)	OSC32_IN	
4	PC15-OSC32_OUT(4)	PC15(5)	OSC32_OUT	
5	OSC_IN	OSC_IN		
6	OSC_OUT	OSC_OUT		
7	NRST	NRST		
8	PC0	PC0	ADC12_IN10	
9	PC1	PC1	ADC12_IN11	
10	PC2	PC2	ADC12_IN12	
11	PC3	PC3	ADC12_IN13	
12	V_{SSA}	V_{SSA}		
13	V_{DDA}	V_{DDA}		
14	PA0-WKUP	PA0	WKUP/USART2_CTS(7) / ADC12_IN0 / TIM2_CH1_ETR(7)	
15	PA1	PA1	USART2_RTS(7) / ADC12_IN1 / TIM2_CH2(7)	
16	PA2	PA2	USART2_TX(7) / ADC12_IN2 / TIM2_CH3(7)	
17	PA3	PA3	USART2_RX(7) / ADC12_IN3 / TIM2_CH4(7)	
18	V_{SS_4}	V_{SS_4}		
19	V_{DD_4}	V_{DD_4}		
20	PA4	PA4	SPI1_NSS(7) / USART2_CK(7) / ADC12_IN4	
21	PA5	PA5	SPI1_SCK(7) / ADC12_IN5	
22	PA6	PA6	SPI1_MISO(7) / ADC12_IN6 / TIM3_CH1(7)	TIM1_BKIN
23	PA7	PA7	SPI1_MOSI(7) / ADC12_IN7 / TIM3_CH2(7)	TIM1_CH1N
24	PC4	PC4	ADC12_IN14	
25	PC5	PC5	ADC12_IN15	
26	PB0	PB0	ADC12_IN8 / TIM3_CH3(7)	TIM1_CH2N
27	PB1	PB1	ADC12_IN9 / TIM3_CH4(7)	TIM1_CH3N
28	PB2 / BOOT1	PB2 / BOOT1		
29	PB10	PB10	I2C2_SCL / USART3_TX(6)(7)	TIM2_CH3
30	PB11	PB11	I2C2_SDA / USART3_RX(6)(7)	TIM2_CH4
31	V_{SS_1}	V_{SS_1}		
32	V_{DD_1}	V_{DD_1}		
33	PB12	PB12	SPI2_NSS(6)/I2C2_SMBAI(6) / USART3_CK(6)(7) / TIM1_BKIN(7)	
34	PB13	PB13	SPI2_SCK(6) / USART3_CTS(6)(7) TIM1_CH1N(7)	
35	PB14	PB14	SPI2_MISO(6) / USART3_RTS(6)(7) TIM1_CH2N(7)	
36	PB15	PB15	SPI2_MOSI(6) / TIM1_CH3N(7)	
37	PC6	PC6		TIM3_CH1

38	PC7	PC7		TIM3_CH2
39	PC8	PC8		TIM3_CH3
40	PC9	PC9		TIM3_CH4
41	PA8	PA8	USART1_CK / TIM1_CH1[7]/MCO	
42	PA9	PA9	USART1_TX[7] / TIM1_CH2[7]	
43	PA10	PA10	USART1_RX[7] / TIM1_CH3[7]	
44	PA11	PA11	USART1_CTS / CANRX[7] / TIM1_CH4[7] / USBDM	
45	PA12	PA12	USART1_RTS / CANTX[7] / TIM1_ETR[7] / USBDP	
46	PA13/JTMS/SWDIO	JTMS/SWDIO	PA13	
47	V_{SS_2}	V_{SS_2}		
48	V_{DD_2}	V_{DD_2}		
49	PA14/JTCK/SWCLK	JTCK/SWCLK	PA14	
50	PA15/JTDI	JTDI	PA15	TIM2_CH1_ETR / SPI1_NSS
51	PC10	PC10		USART3_TX
52	PC11	PC11		USART3_RX
53	PC12	PC12		USART3_CK
5	PD0	OSC_IN[8]		CANRX
6	PD1	OSC_OUT[8]		CANTX
54	PD2	PD2	TIM3_ETR	
55	PB3/JTDO	JTDO	PB3 / TRACESWO	TIM2_CH2 / SPI1_SCK
56	PB4/JNTRST	JNTRST	PB4	TIM3_CH1 / SPI1_MISO
57	PB5	PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
58	PB6	PB6	I2C1_SCL[7] / TIM4_CH1[6][7]	USART1_TX
59	PB7	PB7	I2C1_SDA[7] / TIM4_CH2[6][7]	USART1_RX
60	BOOT0	BOOT0		
61	PB8	PB8	TIM4_CH3[6][7]	I2C1_SCL / CANRX
62	PB9	PB9	TIM4_CH4[6][7]	I2C1_SDA / CANTX
63	V_{SS_3}	V_{SS_3}		
64	V_{DD_3}	V_{DD_3}		

(주석)

* 4. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.

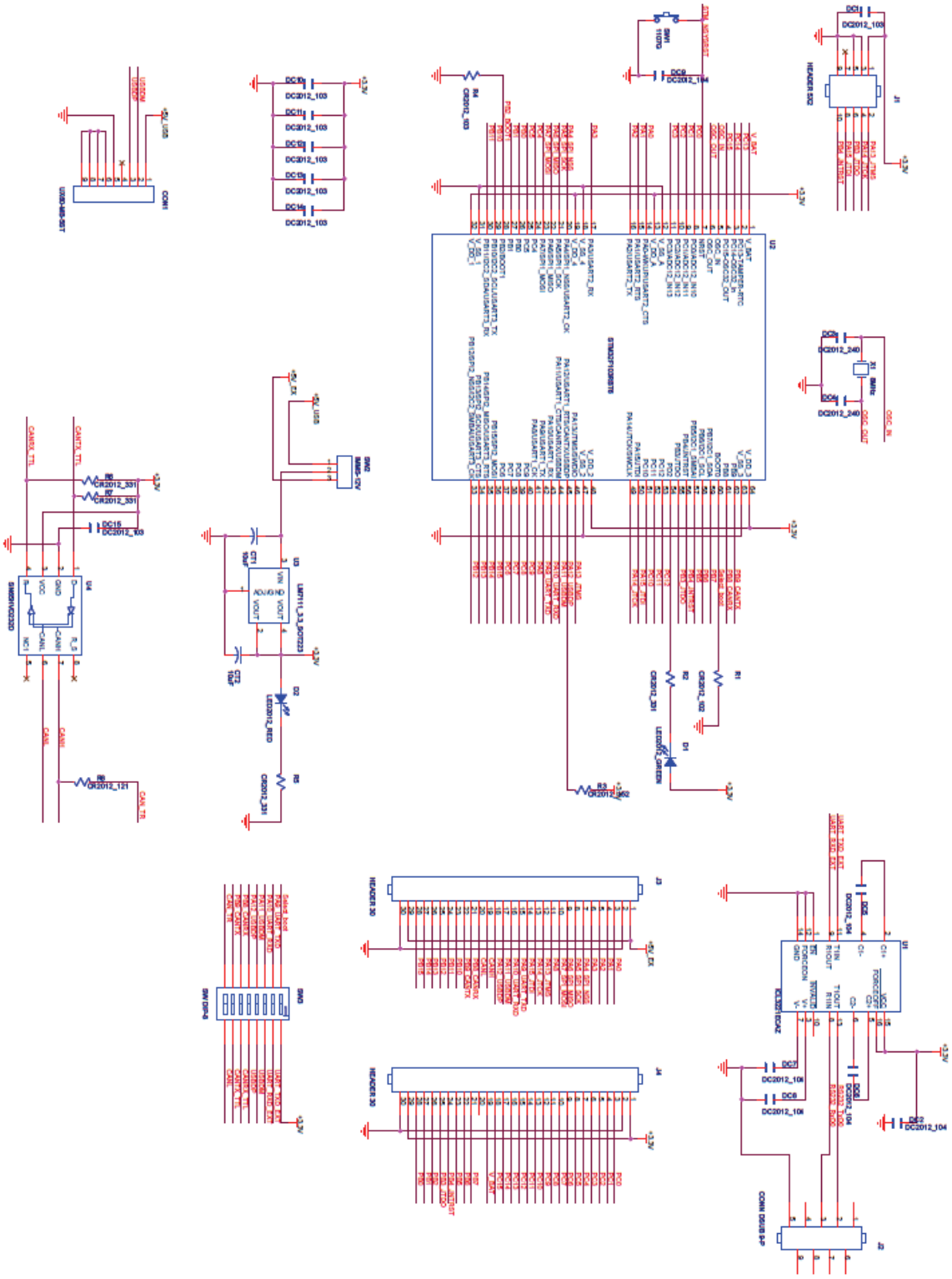
* 5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

* 6. Available only on devices with a Flash memory density equal or higher than 64 Kbytes.

* 7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

* 8. The pins number 2 and 3 in the VFQFPN36 package, and 5 and 6 in the LQFP48 and LQFP64 packages are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual. The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

7. Schematic



* M2CV 홈페이지 다운로드에 Cortex-M3-V3_SCHEMATIC.pdf 파일 참조