PS311DVS Datasheet

Digital Proximity Sensor with I2C Interface and VCSEL

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SNA Co., Ltd.

ENGINEERING CHANGE NOTICE:

Number	Data	Version	Modify	Modify the content
1	2021 - 11 - 29	V 1 . 01	K. Park	Create a new specification
2				
3				
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1. Description

The PS311DVS has full proximity sensing features in a 4.0mm x 2.4mm tiny package including 850nm VCSEL as a light source.
The programmable proximity detection parameters of PS311DVS satisfy various proximity detection demands. (eg. close/away event detection)
Internal state machine provides the device the ability to put the device into a low power mode to save power for battery powered applications.

2. Features

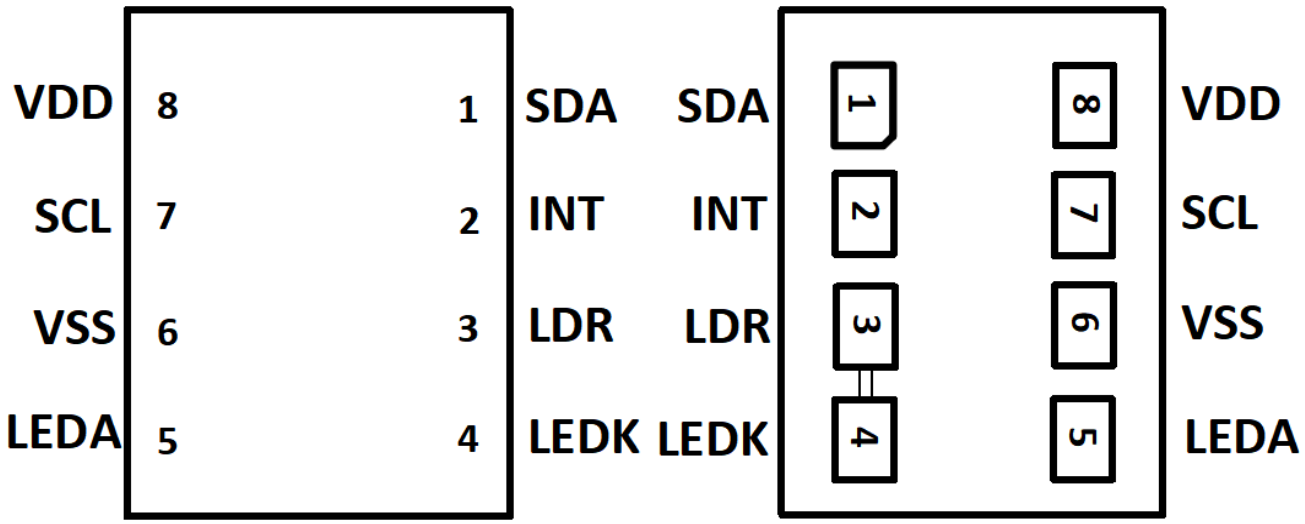
- Full proximity sensor feature in tiny package size
  - 4.0mm x 2.4mm x 1.35mm
  - 16-bit ADC
  - Integrated 850nm 210mw VCSEL
- Programmable Proximity Detection and Interrupt
  - Programmable ADC, LED driver parameters
  - Programmable Interrupt generation conditions
- I2C Interface Compatible
  - Up to 400kHz (I2C Fast Mode)
  - OTP select able device address. : 0x39, 0x3D (7bit)
  - I2C H-level range: 1.8V to 5V
- Power Management
  - Supply voltage range: 2.5V to 5V
  - Low Power 1uA Sleep State
  - 70uA Wait State with Programmable Wait Time

3. Applications

- Contact less devices (dispenser, thermometer)
- TWS(True Wireless Stereo) blue tooth headset
- Other wearable devices

PRODUCT SUMMARY				
Operating Voltage Range [V]	**No. of Connection**	**I2C BUS Voltage Range [V]**	**LED PULSE Current [mA]**	**Output Resolution [bit]**
2.5 to 5	5	1.8 to 5	5 to 125	16

4. Pin Configuration and Functions



[Top View] [Bottom View]

Pin Functions

PIN No	PIN Name	TYPE	DESCRIPTION
1	SDA	I/O	I2C serial data input/output terminal
2	INT	O	Interrupt – open drain (active low)
3	LDR	O	Proximity IR LED controlled current sink driver
4	LEDK	O	Vcsel Diode Cathode
5	LEDA	I	Vcsel Diode Anode
6	VSS	G	Supply Ground
7	SCL	I	I2C serial clock input terminal
8	VDD	P	Supply voltage

5. Specifications

5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Power Supply Voltage	-0.3	6	V
Vin	Input Voltage	-0.3	VDD	V
Vout	Output Voltage	-0.3	VDD	V
Tj	Junction Temperature	-40	125	℃

+ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1: All voltage values are with respect to VSS.

5.2 ESD Ratings

SYMBOL	PARAMETER	VALUE	UNIT
VESD	Human-Body Model (HBM)	+/- 2000	V
	Machine Model (MM)	+/- 200	

5.3 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VDD	Power Supply Voltage	2.5	3.0	5	V
Vin	Input Voltage	0		VDD	V
Vout	Output Voltage	0		VDD	V
TA	Operating ambient temperature	-40		85	℃

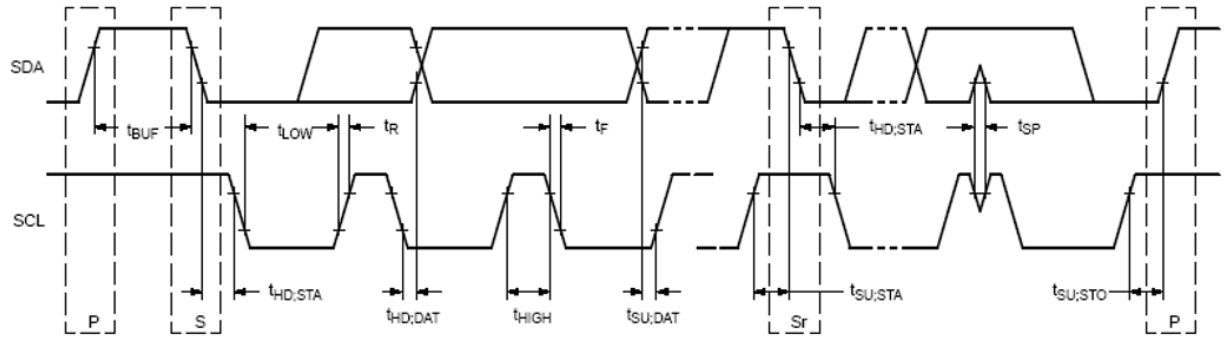
5.4 Electrical Characteristics (VDD = 3V, Ta = 25℃)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current	Active – LDR pulses off		265		uA
	Wait state		55		
	Sleep state		1	10	
	PWIDTH =17.4us, PPULSE=1, PDRIVE=5mA, PTIME=185us, WTIME=4.07ms		75		
Max. Supply Current	PWIDTH =4.4ms, PPULSE=255, PDRIVE=5mA,		2.647		mA
INT, SDA output low voltage	3mA sink current	0		0.4	V
	6mA sink current	0		0.6	
Low Level Input Voltage				0.3VDD	V
High Level Input Voltage		0.7VDD			V

+ External pull-up voltage on I2C and INT lines can be lower than VDD.
  Lower IO pull-up voltage must be decided considering VDD voltage level.

5.5 Data Transmission Timing Requirements

PARAMETER	Symbol	CONDITIONS	MIN	MAX	UNIT
Output Low Level (SDA)	V_{OL}	IOL = 4mA		0.5	V
SCLK Operating Frequency	f_{SCLK}			400	kHz
Stop and Start Condition	t_{BUF}		1.3		us
Hold Time After Repeated Start Conditions	$t_{HD;STA}$		0.6		us
SCLK Clock Low Period	t_{LOW}		1.3		us
SCLK Clock High Period	t_{HIGH}		0.6		us
Repeated Start Condition Setup Time	$t_{SU;STA}$		0.6		us
Data Hold Time	$t_{HD;DAT}$		0	0.9	us
Data Setup Time	$t_{SU;DAT}$		100		ns
Clock/Data Fall Time	t_F			300	ns
Clock/Data Rise Time	t_R			300	ns
Stop Condition Setup Time	$t_{SU;STO}$		0.6		us



5.6 Proximity Characteristics (VDD = 3V, Ta = 25℃, PEN = 1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Prox. Full count value					65535	counts
LED drive current	PDH = 0	PDRIVE = 0		125		mA
		PDRIVE = 1		100		
		PDRIVE = 2		75		
		PDRIVE = 3		50		
	PDH = 1	PDRIVE = 0		12.5		mA
		PDRIVE = 1		10		
		PDRIVE = 2		7.5		
		PDRIVE = 3		5		
Prox. offset	PDRIVE = 0				4	counts

5.7 Electro-Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Optical Output Power	CW, 7.0mA 25℃	5	6	-	mW
Operating Current	CW, 25℃	-	7	-	mA
Power Conversion Efficiency	CW, 7.0mA 25℃	38	41	-	%
Wavelength	CW, 7.0mA 25℃	840	850	860	

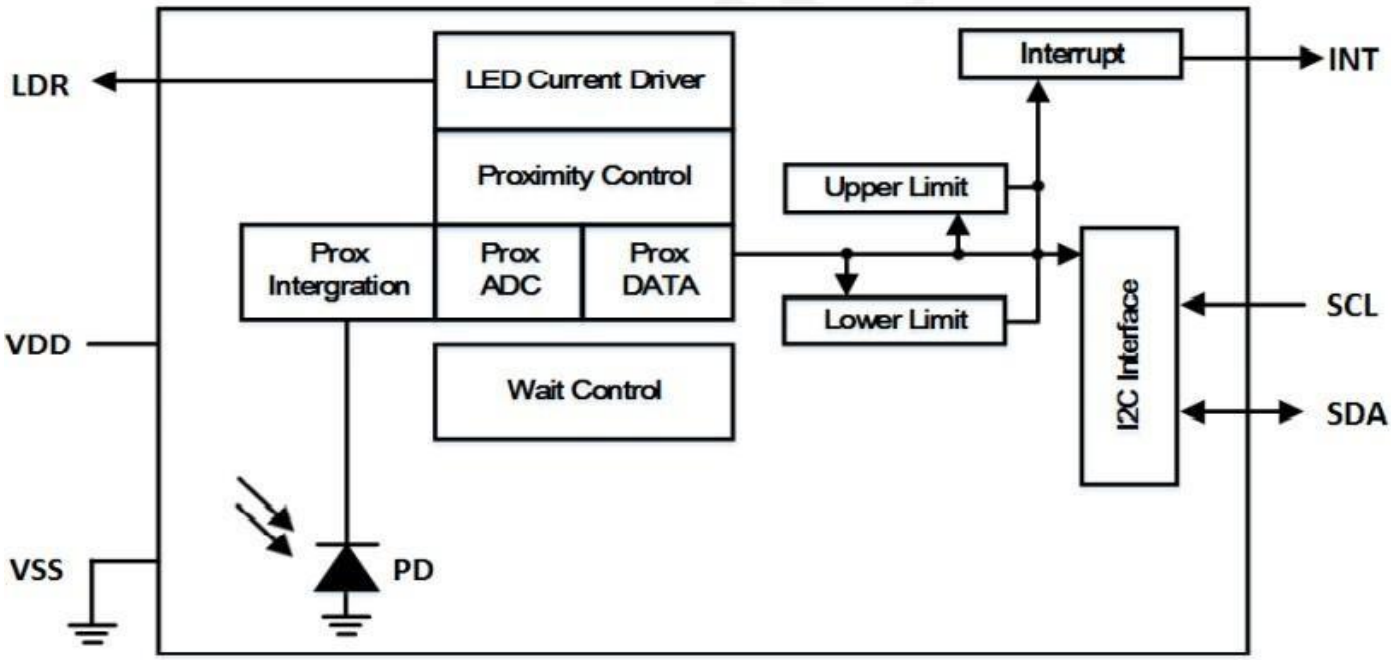
6. Detailed Description

6.1 Overview

The PS311DVS provides on-chip photo diode, integrating amplifier, ADC, accumulator, clock, buffer, comparator, a state machine and an I2C interface. Also It has integrated VCSEL as a light source. Integrating ADC simultaneously convert the amplified photo diode currents into a digital value providing up to 16 bits of resolution.

The I2C interface which supports up to 400-kbits/s data rate. The digital interface of this IC operates between 1.8V and 5.0V.

These features makes PS311DVS can be programmed for using in various applications



<Functional Block Diagram>

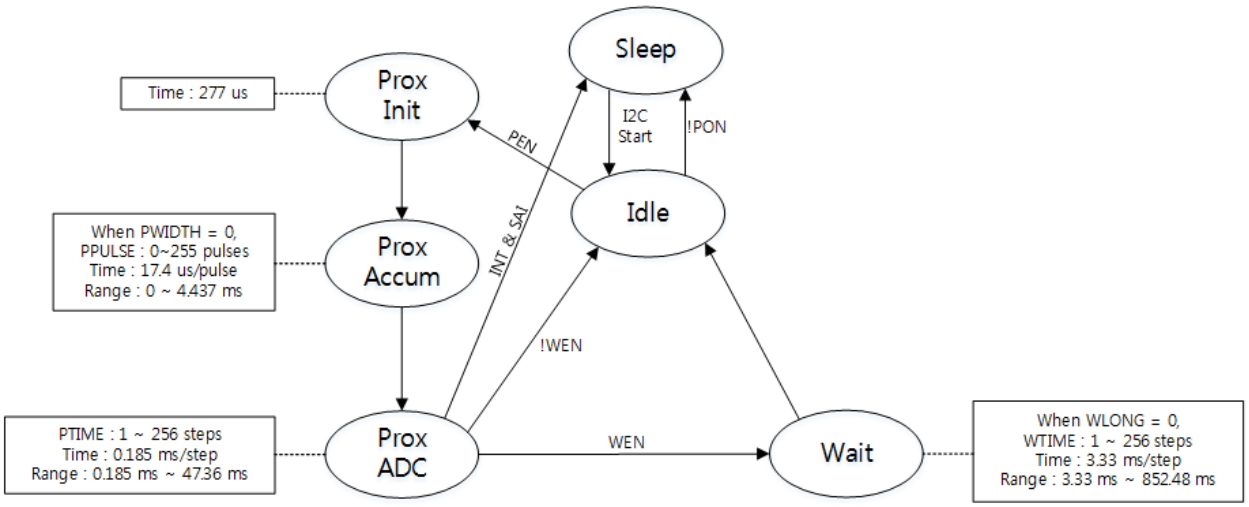
6.2 Feature Description

6.2.1 System State machine

An internal state machine provides system control of the proximity detection, power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected via the I2C bus, the device changes its state to the Idle state where it checks the Enable register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a proximity function is enabled. Once PON is enabled, the device will execute the proximity detection sequence consists of three states of proximity. If WEN is enabled, the proximity. states is followed by Wait state as shown in Figure

1. Upon completion and return to Idle, the device will automatically begin a new proximity-wait cycle as long as PON and PEN remain enabled.

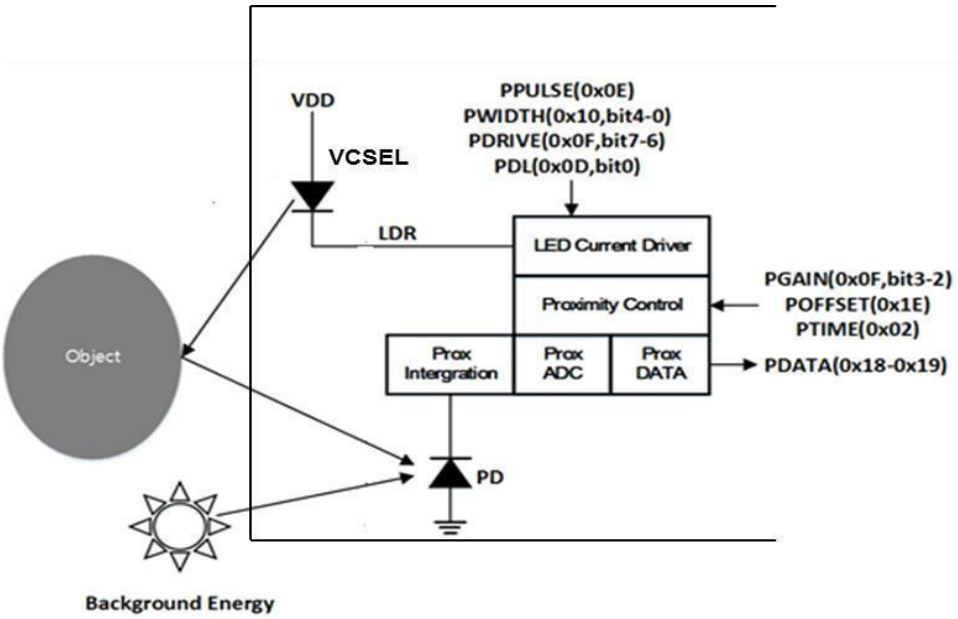


PON, PEN, WEN and SAI are fields in the ENABLE register (0x00).

<State Diagram>

6.2.2 Proximity Detection

Proximity detection is accomplished by measuring the amount of light energy, generally from an VCSEL, reflected off an object to determine its distance. The proximity light source is driven by the integrated proximity LED current driver as shown in Figure 2.



<Proximity Detection>

The integrated LED current driver is a regulated current sink which doesn't need external current sensing resistor for current control. The LED current driver allows user to set the LED drive current from 5mA to 125mA using a combination of PDRIVE register and PDL bit of CONFIG register.

The integrated current driver and the LED provides external pins, LDR, LDR_LED respectively. To use internal light source, the pins need to be connected to each other. Or to drive an external light source with more than 125mA or to minimize on-chip ground bounce, LDR pin can be used to drive an external p-type transistor which drives external light source.

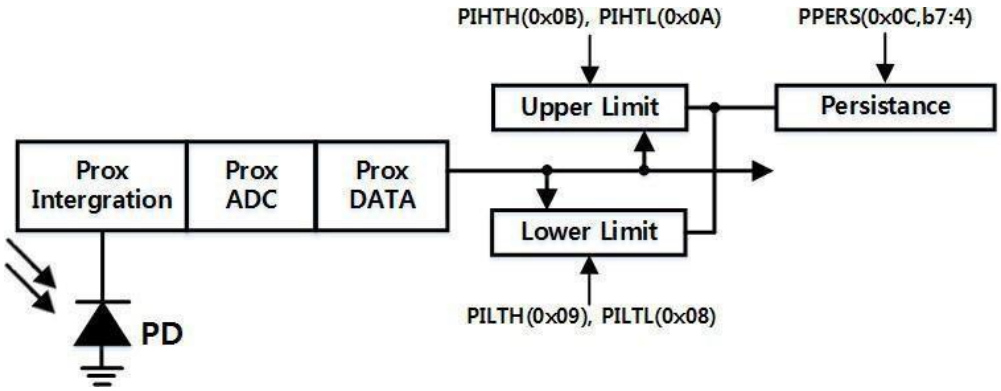
6.2.3 Interrupt

The interrupt feature simplifies and improves system efficiency by eliminating the necessity for polling the sensor to find out whether proximity values are in the outside of user-defined range. While the interrupt function is always enabled and its status is available in the Status register (0x13), the output of the interrupt state can be enabled using the Interrupt Manual Clear Enable (IMCEN) field in the Enable register (0x00). Once IMCEN field is set to 1, interrupt parameters and signal activity of INT pin are need to be controlled via I2C.

Two 16-bit interrupt threshold registers allow the user to set limits below and above a desired VCSEL proximity range. An interrupt can be generated when the proximity data (PDATA) is less than the proximity interrupt low threshold (PILTX) or is greater than the proximity interrupt high threshold (PIHTX).

The device also provides an interrupt persistence feature. The persistence filter allows the user to specify the number of consecutive out-of-range proximity occurrences as an interrupt generation condition. The persistence filter register (0x0C) allows the user to set the proximity persistence filter (PPERS) values. See the persistence filter register for details on the persistence filter values.

Once an interrupt is generated and issued, the interrupt has to be cleared after the service routine has been executed for next interrupt generation. Simply reading the Interrupt clear register performs this interrupt clear operation.



<Programmable Interrupt>

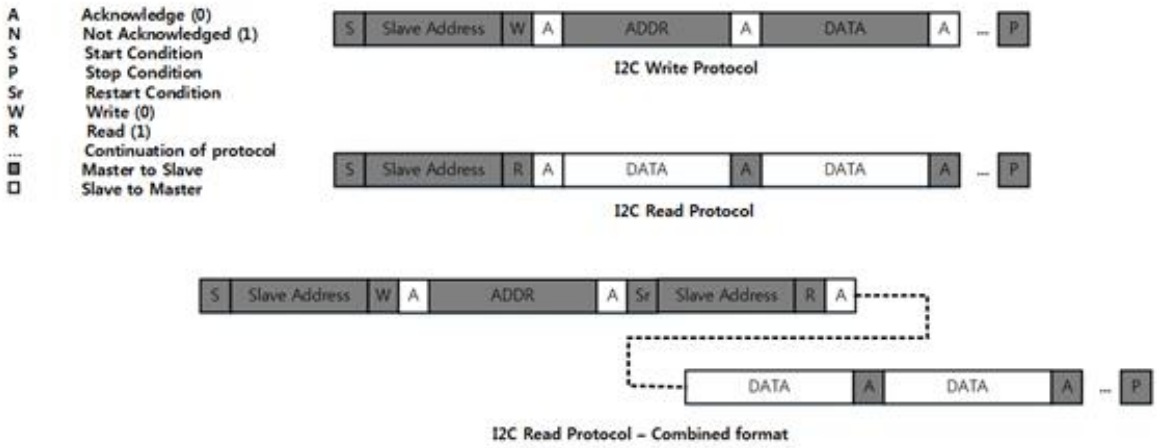
6.3 Programming

6.3.1 I2C Protocol

Interface and control of the PS311DVS is accomplished through an I2C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports OTP select able I2C slave address between 0x39 and 0x3D using 7-bit addressing protocol.

The I2C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 4). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

For a complete description of I2C protocols, please review the I2C Specification at: http://www.semiconductors.philips.com.



< I2C Protocols>

6.4 Register Maps

ADDRESS	NAME	R/W	REGISTER FUNCTION	DEFAULT
-	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	RW	Enable states and interrupts	0x0D
0x02	PTIME	RW	Proximity time	0xFF
0x03	WTIME	RW	Wait time	0xFF
0x08	PILTL	RW	interrupt low threshold low byte	0x80
0x09	PILTH	RW	interrupt low threshold high byte	0x00
0x0A	PIHTL	RW	interrupt high threshold low byte	0x00
0x0B	PIHTH	RW	interrupt high threshold high byte	0x02
0x0C	PPERS	RW	Interrupt persistence filter	0x00
0x0D	CONFIG	RW	Configuration	0x00
0x0E	PPULSE	RW	Pulse count	0x04
0x0F	CONTROL	RW	Control register	0x80
0x10	PWIDTH	RW	Pulse width	0x00
0x12	ID	R	Device ID	0x03
0x13	STATUS	R	Device status	0x00
0x16	T_GAIN	RW	Trim gain	0x00
0x17	T_OFFSET	RW	Trim offset	0x00
0x18	PDATAL	R	Proximity data low byte	0x00
0x19	PDATAH	R	Proximity data high byte	0x00
0x1A	TRIM_EN	RW	Trim register enable	0x00
0x65	INTCLEAR	R	Interrupt clear	0x00

6.4.1 ADDR(COMMAND) Register

The ADDR (COMMAND) register specifies the address of the target register for future read and write operations, as well as issues special function commands.

	7	6	5	4	3	2	1	0	
ADDR	**TYPE**			**ADDR/SF**					**Default 0x00**

FIELD	BITS	DESCRIPTION (Default = 0x00)	
TYPE	7:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**DESCRIPTION**
		000	Repeated byte protocol transaction
		001	Auto-increment protocol transaction
		010	Reserved — Do not use
		011	Special function — See description below
ADDR /SF	4:0	Address field/special function field. The field values listed below apply only to special function commands:	
		FIELD VALUE	**DESCRIPTION**
		00101	interrupt clear
		other	Reserved — Do not use

6.4.2 ENABLE Register (0x00)

The enable register is used to power the device on/off, enable functions, and interrupts.

	7	6	5	4	3	2	1	0
ENABLE	Reserved	SAI	IMCEN	Reserved	WEN	PEN	Reserved	PON

FIELD	BITS	DESCRIPTION (Default = 0x0D)
Reserved	7	Reserved. Write as 0.
SAI	6	Sleep after interrupt. When asserted, the device will power down at the end of a proximity cycle if an interrupt has been generated.
IMCEN	5	Interrupt Manual Clear Enable. When asserted, permits proximity interrupts to be cleared via I2C.
Reserved	4	Reserved. Write as 0.
WEN	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
Reserved	1	Reserved. Write as 0.
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channel to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

6.4.3 PTIME Register (0x02)

The proximity time register controls the integration time of the proximity ADC in 0.185 ms increments. Upon power up, the proximity time register is set to 0xFF. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

FIELD	BITS	DESCRIPTION (Default = 0xFF)		
PTIME	7:0	VALUE	INTEG_CYCLES	TIME
		0xFF	1	0.185 ms
		0xFE	2	0.370 ms
		...	...	...
		0x00	256	47.36 ms

6.4.4 WTIME Register (0x03)

Wait time is set 4.07 ms increments unless the WLONG bit is asserted. When WLONG bit is asserted, the wait times are 10 × longer. WTIME is programmed as a 2's complement number. Upon power up, the wait time register is set to 0xFF.

FIELD	BITS	DESCRIPTION (Default = 0xFF)			
		VALUE	WAIT TIME	TIME(WLONG=0)	TIME(WLONG=1)
WTIME	7:0	0xFF	1	4.07 ms	0.042 sec
		0xFE	2	7.74 ms	0.079 sec
		...	...	...	...
		0x00	256	939.92 ms	9.6 sec

6.4.5 Proximity Interrupt Threshold Registers (0x08 – 0x0B)

The proximity interrupt threshold registers provide the upper and lower threshold values to the proximity interrupt comparators. See Interrupts in the Feature Description section for detailed information and power-on-default values.

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity interrupt low threshold low byte
PILTH	0x09	7:0	Proximity interrupt low threshold high byte
PIHTL	0x0A	7:0	Proximity interrupt high threshold low byte
PIHTH	0x0B	7:0	Proximity interrupt high threshold high byte

6.4.6 Interrupt Persistence Filter Register (0x0C)

The interrupt persistence filter sets the number of consecutive proximity cycles that are out- of-range to generate an interrupt. Out-of-range is determined by the proximity interrupt threshold registers (0x08 through 0x0B). See Interrupts in the Feature Description section for further information. Upon power up, the interrupt persistence filter register resets to 0x00, which will generate an interrupt at the end of each proximity cycle.

	7	6	5	4	3	2	1	0	
PPERS	**PPERS**				**Reserved**				**Default 0x00**

FIELD	BITS	DESCRIPTION (Default = 0x00)	
PPERS	7:4	Proximity persistence. Controls rate of proximity interrupt to the host processor.	
		FIELD VALUE	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every proximity cycle generates an interrupt
		0001	1 proximity value out of range
		0010	2 consecutive proximity values out of range
		...	...
		1111	15 consecutive proximity values out of range
Reserved	3:0	Reserved. Write as 0.	

6.4.7 Configuration Register (0x0D)

The configuration register sets the proximity LED drive level and wait long time.

	7	6	5	4	3	2	1	0	
CONFIG	**Reserved**						**WLONG**	**PDL**	**Default 0x00**

FIELD	BITS	DESCRIPTION (Default = 0x00)
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 10 × from that programmed in the WTIME register.
PDL	0	Proximity drive level. When asserted, the proximity LDR drive current is reduced by 10

6.4.8 Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that the LDR pin will generate during the Proximity Accumulate state.

FIELD	BITS	DESCRIPTION (Default = 0x04)
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses tobegenerated.

6.4.9 Control Register (0x0F)

The control register sets the proximity LED current drive value and gain.

	7	6	5	4	3	2	1	0
CONTROL	PDRIVE		Reserved		PGAIN		Reserved	

FIELD	BITS	DESCRIPTION (Default = 0x80)		
PDRIVE	7:6	Proximity LED Drive Strength.		
		FIELD VALUE	PDL = 0	PDL = 1
		00	125mA	12.5mA
		01	100mA	10mA
		10	75mA	7.5mA
		11	50mA	5.0mA
Reserved	5:4	Reserved. Write as 0.		
PGAIN	3:2	Proximity Gain.		
		FIELD VALUE	PROXIMITY GAIN VAULE	
		00	1X Gain	
		01	2X Gain	
		10	4X Gain	
		11	Reserved	
Reserved	1:0	Reserved. Write as 0.		

6.4.10 Pulse Width Register (0x10)

The pulse width register sets the width of proximity pulses that the LDR pin will generate during the Proximity Accumulate state.

	7	6	5	4	3	2	1	0	
PWIDTH	Reserved				PWIDTH				Default 0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)	
Reserved	7:4	Reserved. Write as 0.	
PWIDH	3:0	Proximity Width. 17.4us x (2 ^ PWIDTH)	
		FIELD VALUE	PROXIMITY PERIOD TIME
		0000	17.4 us
		0001	34.8 us
		0010	69.6 us
		...	...
		1000	4454.4 us
		Reserved	Reserved

6.4.11 ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

FIELD	BITS	DESCRIPTION (Default = 0x03)
ID	7:0	Part number identification : 0x03 = SO6103

6.4.12 STATUS Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

	7	6	5	4	3	2	1	0	
STATUS	Reserved		PINT	Reserved			PVALID	Reserved	Default 0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)
Reserved	7:6	Reserved. Read as 0.
PINT	5	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.
Reserved	4:2	Reserved. Read as 0.
PVALID	1	Proximity Valid. Indicates that the proximity channel has completed an integration cycle after PEN has been asserted
Reserved	0	Reserved. Read as 0.

6.4.13 Proximity Data Registers (0x18 – 0x19)

Proximity data is stored as a 16-bit value. The simplest way to read both bytes is to perform a two-byte I2C read operation using the auto-increment protocol, which is set in the ADDR register TYPE field.

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

6.4.14 Trim Gain Register (0x16)

The Trim gain Register can control analog gain. One step can change about 1.8%. It only works when T_GAIN_EN(0x1A) is high.

Trim Gain

7	6	5	4	3	2	1	0	Default
Reserved		TRIM_GAIN						0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)
Reserved	7:6	Reserved. Read as 0.
TRIM_GAIN	5:0	Analog gain Trimming 6bit (0~63).

6.4.15 Trim Offset Register (0x17)

The Trim offset Register can control analog offset. One step can change about -13Code(@PTIME 370us).

Trim offset depends on the PTIME setting. It only works when T_OFFSET_EN(0x1A) is high.

Trim Offset

7	6	5	4	3	2	1	0	Default
Reserved		TRIM_OFFSET						0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)
Reserved	7:6	Reserved. Read as 0.
TRIM_OFFSET	5:0	Analog offset Trimming 6bit (0~63).

6.4.16 Trim Enable Register (0x1A)

A user can activate user trim values which are stored to Trim Gain Register and Trim Offset Register to apply them to operation.

When the each enable bits are set, sensor refers the Trim Gain Register and Trim Offset Register instead of trim bits of OTP.

	7	6	5	4	3	2	1	0	
Trim Enable	Reserved						T_GAIN_EN	T_OFFSET_EN	Default 0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)
Reserved	7:2	Reserved.
T_GAIN_EN	1	Applying Trim Gain Register to operation.
T_OFFSET_EN	0	Applying Trim Offset Register to operation.

6.4.17 Interrupt clear Register (0x65)

Interrupts are cleared by reading to the Interrupt clear Register(0x65). Ex)

I2C_Read Byte(0x72, 0x65); // read interrupt clear

I2C_Read Byte(0x72, 0x13); // read status

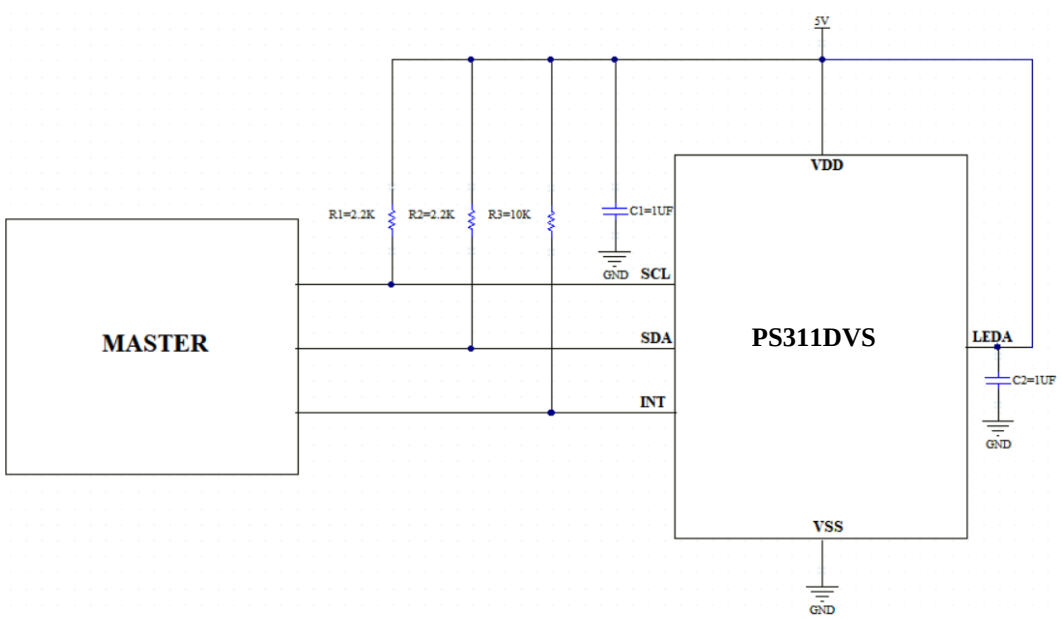
7. Application

7.1 Typical Application

In a proximity sensing system, the VCSEL can be pulsed by the PS311DVS with up to 125 MA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key of goal is to reduce the power supply noise coupled back into the device during the LED pulse.

C1 should be placed as close as possible to the IC. And bulk capacitance, C2 might to be required in case. C2 can be placed far from the IC than C1 but, higher capacitance than 2.2uF is required.

Typical values of the pull-up resistors are 2.2k ohm and 10k ohm respectively. Generally, VDD_IO and VDD are same. In case of lower I2C and IO voltage than VDD are required, user can separate VDD_IO and VDD.



8. Package Dimension