

## 1. INTRODUCTION

- Digital MEMS Microphone - ½ Cycle PDM 16bit, Full Scale=120dB SPL
- Bottom Port Type – Sensitivity is Typical -26dBFS at LPM and STM
- **High Signal to Noise Ratio(SNR) – Typical 64.5dB (A-weighted, 20Hz~20kHz) at fclk=2.4MHz**
- **Multiple Clock Mode – Stand by Mode, Low-Power Mode(LPM), Standard Mode(STM)**
- **Narrow Sensitivity – +/-1dB**
- Omni-directional
- Dual Channel supported
- RF Shielded – with embedded Capacitor
- Compatible with Sn/Pb and Halogen-free solder process
- RoHS compliant
- SMD reflow temperature of up to 260°C for over 30 seconds



## 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Absolute maximum rating	Units
Vdd , Data to Ground	3.6	V
Clock to Ground	3.6	V
Select to Ground	3.6	V
Input Current	2	mA
Short Circuit Current to/from Data	Infinite to Ground or Vdd	sec

## 3. GENERAL MICROPHONE SPECIFICATIONS

Test Condition : 23 ± 2°C, Room Humidity = 55 ± 20 %, Vdd=1.8V, fclk = 2.4MHz, SELECT Pin is grounded, CLOAD = 1μF, unless otherwise noticed

Parameter	Conditions	Min	Typ	Max	Units	
* Clock Frequency Range	Stand by Mode	Max. Tolerance ±5%	0	-	350	kHz
	Low-Power Mode	Generally at ±10% of typical value	450	768	850	kHz
	Standard Mode	Generally at ±10% of typical value	1.38	1.536	1.7	MHz
			2.1	2.4	2.6	
		2.9	3.072	3.3		
Standby Mode Current	fCLK < 350kHz	-	25	50	μA	
Short Circuit Current	Grounded DATA pin	1	-	20	mA	
Clock off Mode Current	Clock pulled low	-	<1	35	μA	
Vdd Ramp-up Time (Power-up)	Vdd ≥ Vdd (min)	-	-	50	ms	
Startup Time	Time to start up in any mode after VDD and CLOCK applied	-	-	50	ms	
Reset Time	Time to start up in any mode after VDD has been off for more than 10ms, while CLOCK remained on	-	-	50	ms	
Mode-Change Time	Time to switch between modes. VDD remains on during the mode switch	-	-	50	ms	

\* Note : Must be consulted when used another clock frequency without the typical clock frequencies.

## 4. ABSOLUTE MAXIMUM RATINGS

Parameter	Absolute maximum rating	Units
Vdd , Data to Ground	3.6	V
Clock to Ground	3.6	V
Select to Ground	3.6	V
Input Current	2	mA
Short Circuit Current to/from Data	Infinite to Ground or Vdd	sec

Caution : Stresses above those listed in “Absolute maximum ratings” may cause permanent damage to the device.

These are stress ratings only. Functional operation at these or any other conditions beyond those indicated under “ELECTRO-ACOUSTIC CHARACTERISTICS” is not implied. Exposure beyond those indicated under “ELECTRO-ACOUSTIC CHARACTERISTICS” for extended periods may affect device reliability.

## 5. GENERAL MICROPHONE SPECIFICATIONS

Test Condition :  $23 \pm 2^{\circ}\text{C}$ , Room Humidity =  $55 \pm 20\%$ , Vdd=1.8V, fclk = 2.4MHz, SELECT Pin is grounded, CLOAD =  $1\mu\text{F}$ , unless otherwise noticed

Parameter	Conditions	Min	Typ	Max	Units	
* Clock Frequency Range	Stand by Mode	Max. Tolerance $\pm 5\%$	0	-	350	kHz
	Low-Power Mode	Generally at $\pm 10\%$ of typical value	450	768	850	kHz
	Standard Mode	Generally at $\pm 10\%$ of typical value	1.38	1.536	1.7	MHz
2.1			2.4	2.6		
		2.9	3.072	3.3		
Standby Mode Current	fCLK < 350kHz	-	25	50	$\mu\text{A}$	
Short Circuit Current	Grounded DATA pin	1	-	20	mA	
Clock off Mode Current	Clock pulled low	-	<1	35	$\mu\text{A}$	
Vdd Ramp-up Time (Power-up)	Vdd $\geq$ Vdd (min)	-	-	50	ms	
Startup Time	Time to start up in any mode after VDD and CLOCK applied	-	-	50	ms	
Reset Time	Time to start up in any mode after VDD has been off for more than 10ms, while CLOCK remained on	-	-	50	ms	
Mode-Change Time	Time to switch between modes. VDD remains on during the mode switch	-	-	50	ms	

\* Note : Must be consulted when used another clock frequency without the typical clock frequencies.

## 6. ELECTRO-ACOUSTIC CHARACTERISTICS

Test Condition :  $23 \pm 2^{\circ}\text{C}$ , Room Humidity =  $55 \pm 20\%$ ,  $V_{dd}=1.8\text{V}$ ,  $f_{clk} = 2.4\text{MHz}$ , SELECT Pin is grounded,  $C_{LOAD} = 1\mu\text{F}$ , unless otherwise noticed

Parameter	Conditions	Min	Typ	Max	Units
Directivity		Omni-directional			
Supply Voltage (Vdd)		1.62	-	3.6	V
Sensitivity Change across Voltage	$V_{dd}=1.62\sim 3.6\text{V}$ , $f_{clk}=2.4\text{MHz}$	No change			dB
Data Format		1/2 Cycle PDM 16bit			-
Full Scale Acoustic Level		120			dB SPL
Current Consumption (Idd)	$f_{clk} = 1.536\text{MHz}$ , load on DATA output	490	-	690	$\mu\text{A}$
	$f_{clk} = 2.4\text{MHz}$ , load on DATA output	640	-	840	
	$f_{clk} = 3.072\text{MHz}$ , load on DATA output	760	-	960	

### ● Standard Mode

Test Conditions : Measurement Clock Frequency=2.4MHz,  $V_{dd}=1.8\text{V}$

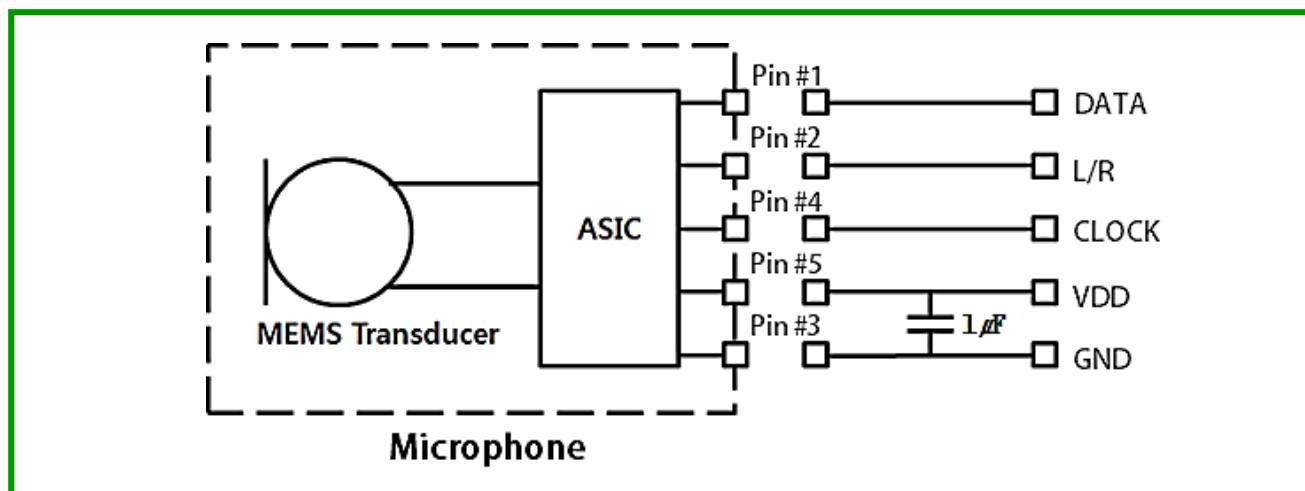
Sensitivity	94dB SPL at 1kHz	-27	-26	-25	dBFS
Signal to Noise Ratio (SNR)	94dB SPL at 1kHz, A-weighted (20Hz~20kHz)	-	64.5	-	dB(A)
Equivalent Input Noise (EIN)	94dB SPL at 1kHz, A-weighted (20Hz~20kHz)	-	29.5	-	dB(A)SPL
Total Harmonic Distortion (THD)	94dB SPL at 1kHz	-	-	0.4	%
	103dB SPL at 1kHz	-	-	1.0	%
	117dB SPL at 1kHz	-	-	5.0	%
Acoustic Overload Point (AOP)	THD>10%, at 1kHz	120	121	-	dB SPL
Power Supply Rejection Ratio (PSRR)	Measured with 1kHz sine wave and broad band noise, both 200mVpp	-	52	-	dBV/FS
Power Supply Rejection (PSR)	Measured with 217Hz square wave and broad band noise, both 100mVpp, A-weighted	-	-84	-	dBFS(A)

### ● Low Power Mode

Test Conditions : Measurement Clock Frequency=768kHz,  $V_{dd}=1.8\text{V}$

Current consumption (Idd)	load on DATA output	180	-	380	$\mu\text{A}$
Sensitivity	94dB SPL at 1kHz	-27	-26	-25	dBFS
Signal to Noise Ratio (SNR)	94dB SPL at 1kHz, A-weighted (20Hz~8kHz)	-	63.5	-	dB(A)
Equivalent Input Noise (EIN)	94dB SPL at 1kHz, A-weighted (20Hz~8kHz)	-	30.5	-	dB(A)SPL
Total Harmonic Distortion (THD)	94dB SPL at 1kHz	-	-	0.4	%
	103.5dB SPL at 1kHz	-	-	1.0	%
	116.5dB SPL at 1kHz	-	-	5.0	%
Acoustic Overload Point (AOP)	THD>10%, at 1kHz	119	120	-	dB SPL
Power Supply Rejection Ratio (PSRR)	Measured with 1kHz sine wave and broad band noise, both 200mVpp	-	52	-	dBV/FS
Power Supply Rejection (PSR)	Measured with 217Hz square wave and broad band noise, both 100mVpp, A-weighted	-	-84	-	dBFS(A)

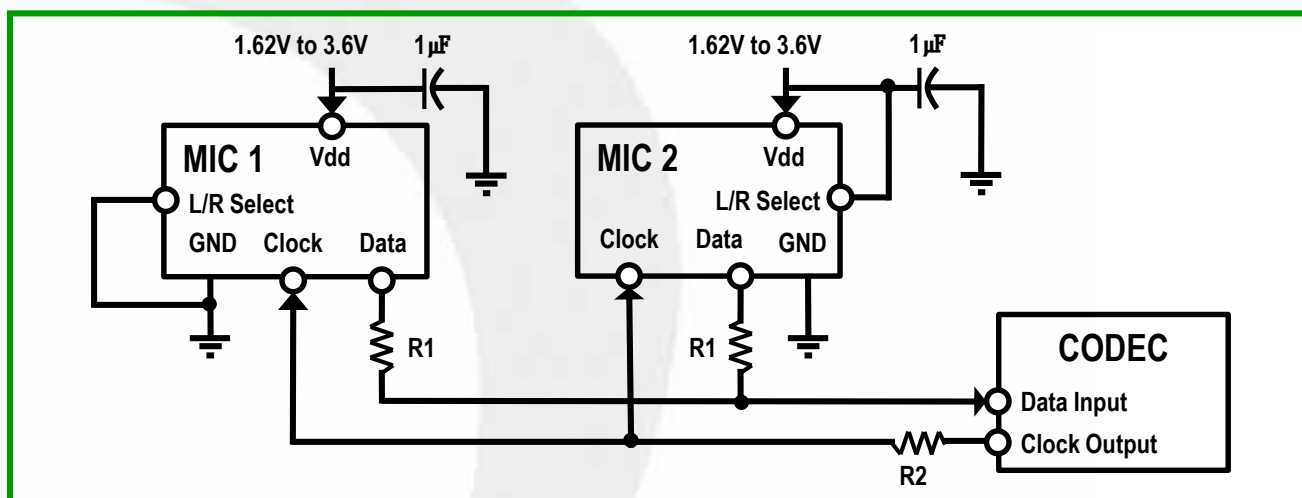
## 7. MEASUREMENT CIRCUIT



## 8. PIN DESCRIPTION

Pin Name	Description
Vdd	Supply and IO voltage for the microphone
L/R Select	Left/Right ( DATA2 / DATA1 ) Channel selection
CLOCK	Clock input to the microphone
DATA	PDM data output from the microphone
GND	Ground

## 9. INTERFACE CIRCUIT & CHANNEL DATA CONFIGURATION



Data symbol in interface timing chart	L/R Select connected to	Data asserted at	Data sampled at
DATA1 [MIC1(Low)]	GND	Falling clock edge	Rising clock edge
DATA2 [MIC2(High)]	Vdd	Rising clock edge	Falling clock edge

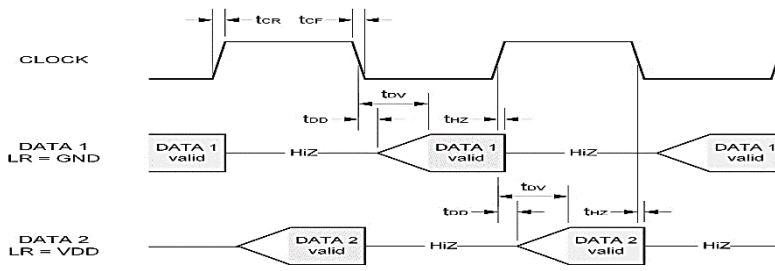
Note 1 : Stereo operation is accomplished by connecting the L/R Sel. pin either to Vdd or GND on the phone PWB.

Bypass Capacitors near each MIC. on Vdd are recommended to provide maximum SNR performance.

Note 2 : R1(Data source termination Resister) should be as close as possible to each the MIC. (50Ω~100Ω)

Note 3 : R2(Clock source termination Resister) should be as close as possible to the CODEC. (50Ω~100Ω)

### 10. INTERFACE TIMING CHART

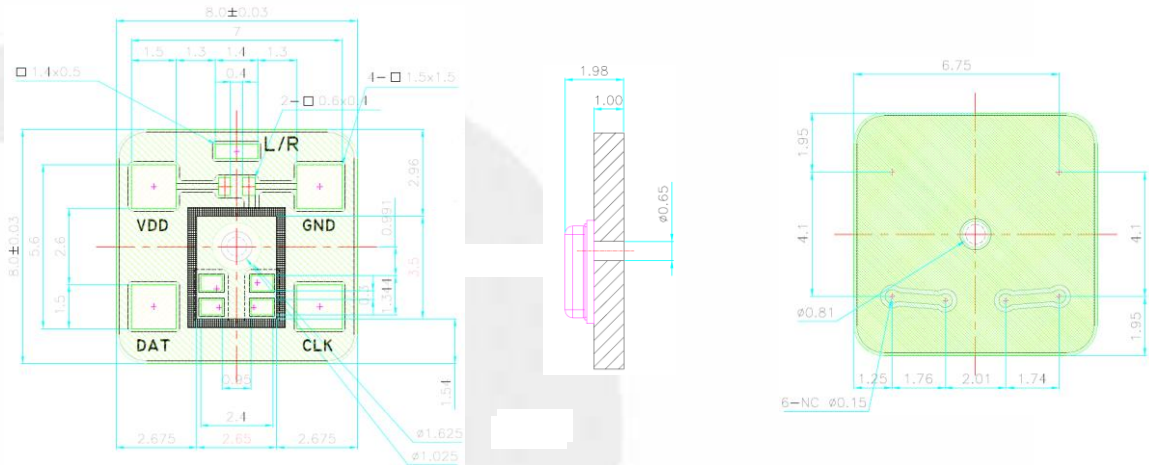


With defining a minimum value for  $t_{dd}$  and a maximum value for  $t_{hz}$  it is secured that the driven DATA signals of the right and the left channel don't overlap. A definition of a maximum value for  $t_{dd}$  is not necessary, instead  $t_{ov}$  defines the time until the driven DATA is valid.

### 11. MECHANICAL CHARACTERISTICS

- Mechanical dimensions & Pad Lay-out

#### Dimensions (Unit : mm)



TOP VIEW

SIDE VIEW

BOTTOM VIEW

Pin #	Pin Name	Type	Description
1	DATA	Digital O	PDM data output
2	L/R	L/R Select	Left/Right channel selection
3	GND	Ground	Ground
4	CLK	Clock	Clock input
5	VDD	Power	Supply and I/O voltage

**Note :** All ground Pins must be connected to ground.  
 "3" Pin must be sealed by solder paste on the PWB.  
 General Tolerance  $\pm 0.08\text{mm}$ .