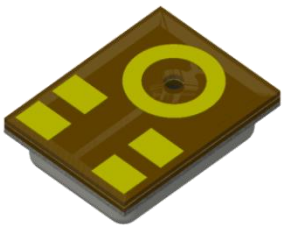
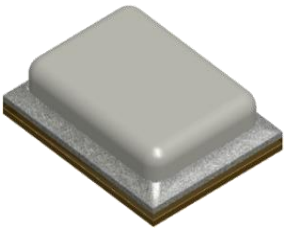
1. INTRODUCTION





- Digital MEMS Microphone - ½ Cycle PDM 16bit, Full Scale=120dBSPL
- Bottom Port Type – Sensitivity is Typical -26dBFS at LPM and STM
- **High Signal to Noise Ratio(SNR) – Typical 64.5dB (A-weighted, 20㎐~20㎑) at fclk=2.4㎒**
- **Multiple Clock Mode – Stand by Mode, Low-Power Mode(LPM), Standard Mode(STM)**
- **Narrow Sensitivity – +/-1dB**
- Omni-directional
- Dual Channel supported
- RF Shielded – with embedded Capacitor
- Compatible with Sn/Pb and Halogen-free solder process
- RoHS compliant
- SMD reflow temperature of up to 260℃ for over 30 seconds

2. ABSOLUTE MAXIMUM RATINGS

Parameter	Absolute maximum rating	Units
Vdd , Data to Ground	**3.6**	V
Clock to Ground	**3.6**	V
Select to Ground	**3.6**	V
Input Current	**2**	mA
Short Circuit Current to/from Data	**Infinite to Ground or Vdd**	sec

3. GENERAL MICROPHONE SPECIFICATIONS

Test Condition : 23 ± 2℃, Room Humidity = 55 ± 20 %, Vdd=1.8V, fclk = 2.4㎒, SELECT Pin is grounded, CLOAD = 1㎌, unless otherwise noticed

Parameter		Conditions	Min	Typ	Max	Units
*** Clock Frequency Range**	**Stand by Mode**	Max. Tolerance ±5%	**0**	**-**	**350**	㎑
	Low-Power Mode	Generally at ±10% of typical value	**450**	**768**	**850**	㎑
	Standard Mode	Generally at ±10% of typical value	**1.38**	**1.536**	**1.7**	㎒
			2.1	**2.4**	**2.6**	
			2.9	**3.072**	**3.3**	
Standby Mode Current		f_{CLK} < 350㎑	**-**	**25**	**50**	㎂
Short Circuit Current		Grounded DATA pin	**1**	**-**	**20**	㎃
Clock off Mode Current		Clock pulled low	**-**	**<1**	**35**	㎂
Vdd Ramp-up Time (Power-up)		Vdd ≥ Vdd (min)	**-**	**-**	**50**	㎳
Startup Time		Time to start up in any mode after VDD and CLOCK applied	**-**	**-**	**50**	㎳
Reset Time		Time to start up in any mode after VDD has been off for more than10ms, while CLOCK remained on	**-**	**-**	**50**	㎳
Mode-Change Time		Time to switch between modes. VDD remains on during the mode switch	**-**	**-**	**50**	㎳

*** Note : Must be consulted when used another clock frequency without the typical clock frequencys.**

4. ABSOLUTE MAXIMUM RATINGS

Parameter	Absolute maximum rating	Units
Vdd , Data to Ground	**3.6**	V
Clock to Ground	**3.6**	V
Select to Ground	**3.6**	V
Input Current	**2**	mA
Short Circuit Current to/from Data	**Infinite to Ground or Vdd**	sec

Caution : Stresses above those listed in “Absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation at these or any other conditions beyond those indicated under “ELECTRO-ACOUSTIC CHARACTERISTICS” is not implied. Exposure beyond those indicated under “ELECTRO-ACOUSTIC CHARACTERISTICS” for extended periods may affect device reliability.

5. GENERAL MICROPHONE SPECIFICATIONS

Test Condition : 23 ± 2℃, Room Humidity = 55 ± 20 %, Vdd=1.8V, fclk = 2.4㎒, SELECT Pin is grounded, CLOAD = 1㎌, unless otherwise noticed

Parameter		Conditions	Min	Typ	Max	Units
*** Clock Frequency Range**	**Stand by Mode**	Max. Tolerance ±5%	**0**	**-**	**350**	㎑
	Low-Power Mode	Generally at ±10% of typical value	**450**	**768**	**850**	㎑
	Standard Mode	Generally at ±10% of typical value	**1.38**	**1.536**	**1.7**	㎒
			2.1	**2.4**	**2.6**	
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Standby Mode Current		f_{CLK} < 350㎑	**-**	**25**	**50**	㎂
Short Circuit Current		Grounded DATA pin	**1**	**-**	**20**	㎃
Clock off Mode Current		Clock pulled low	**-**	**<1**	**35**	㎂
Vdd Ramp-up Time (Power-up)		Vdd ≥ Vdd (min)	**-**	**-**	**50**	㎳
Startup Time		Time to start up in any mode after VDD and CLOCK applied	**-**	**-**	**50**	㎳
Reset Time		Time to start up in any mode after VDD has been off for more than10ms, while CLOCK remained on	**-**	**-**	**50**	㎳
Mode-Change Time		Time to switch between modes. VDD remains on during the mode switch	**-**	**-**	**50**	㎳

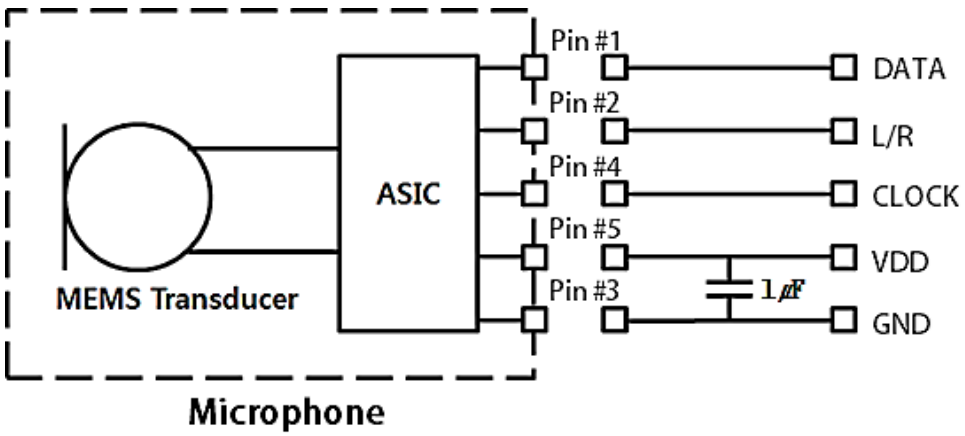
*** Note : Must be consulted when used another clock frequency without the typical clock frequencys.**

6. ELECTRO-ACOUSTIC CHARACTERISTICS

Test Condition : 23 ± 2℃, Room Humidity = 55 ± 20 %, Vdd=1.8V, fclk = 2.4㎒, SELECT Pin is grounded, CLOAD = 1㎌, unless otherwise noticed

Parameter	Conditions	Min	Typ	Max	Units
Directivity		Omni-directional			
Supply Voltage (Vdd)		**1.62**	**-**	**3.6**	V
Sensitivity Change across Voltage	Vdd=1.62~3.6V, fclk=2.4㎒	**No change**			dB
Data Format		**½ Cycle PDM 16bit**			-
Full Scale Acoustic Level			**120**		dBSPL
Current Consumption (Idd)	fclk = 1.536㎒, load on DATA output	**490**	**-**	**690**	µA
	fclk = 2.4㎒, load on DATA output	**640**	**-**	**840**	
	fclk = 3.072㎒, load on DATA output	**760**	**-**	**960**	
● **Standard Mode** **Test Conditions : Measurement Clock Frequency=2.4MHz, Vdd=1.8V**					
Sensitivity	94dB SPL at 1㎑	**-27**	**-26**	**-25**	dBFS
Signal to Noise Ratio (SNR)	94dBSPL at 1㎑, A-weighted (20㎐~20㎑)	**-**	**64.5**	**-**	dB(A)
Equivalent Input Noise (EIN)	94dBSPL at 1㎑, A-weighted (20㎐~20㎑)	**-**	**29.5**	**-**	dB(A)SPL
Total Harmonic Distortion (THD)	94dBSPL at 1㎑	**-**	**-**	**0.4**	%
	103dBSPL at 1㎑	**-**	**-**	**1.0**	%
	112.5dBSPL at 1㎑	**-**	**-**	**3.0**	%
	117dBSPL at 1㎑	**-**	**-**	**5.0**	%
Acoustic Overload Point (AOP)	THD>10%, at 1㎑	**120**	**121**	**-**	dBSPL
Power Supply Rejection Raito (PSRR)	Measured with 1㎑ sine wave and broad band noise, both 200mVpp	**-**	**52**	**-**	dBV/FS
Power Supply Rejection (PSR)	Measured with 217㎐ square wave and broad band noise, both 100mVpp, A-weighted	**-**	**-84**	**-**	dBFS(A)
● **Low Power Mode** **Test Conditions : Measurement Clock Frequency=768kHz, Vdd=1.8V**					
Current consumption (Idd)	load on DATA output	**180**	**-**	**380**	µA
Sensitivity	94dB SPL at 1㎑	**-27**	**-26**	**-25**	dBFS
Signal to Noise Ratio (SNR)	94dBSPL at 1㎑, A-weighted (20㎐~8㎑)	**-**	**63.5**	**-**	dB(A)
Equivalent Input Noise (EIN)	94dBSPL at 1㎑, A-weighted (20㎐~8㎑)	**-**	**30.5**	**-**	dB(A)SPL
Total Harmonic Distortion (THD)	94dBSPL at 1㎑	**-**	**-**	**0.4**	%
	103.5dBSPL at 1㎑	**-**	**-**	**1.0**	%
	112.5dBSPL at 1㎑	**-**	**-**	**3.0**	%
	116.5dBSPL at 1㎑	**-**	**-**	**5.0**	%
Acoustic Overload Point (AOP)	THD>10%, at 1㎑	**119**	**120**	**-**	dBSPL
Power Supply Rejection Raito (PSRR)	Measured with 1㎑ sine wave and broad band noise, both 200mVpp	**-**	**52**	**-**	dBV/FS
Power Supply Rejection (PSR)	Measured with 217㎐ square wave and broad band noise, both 100mVpp, A-weighted	**-**	**-84**	**-**	dBFS(A)

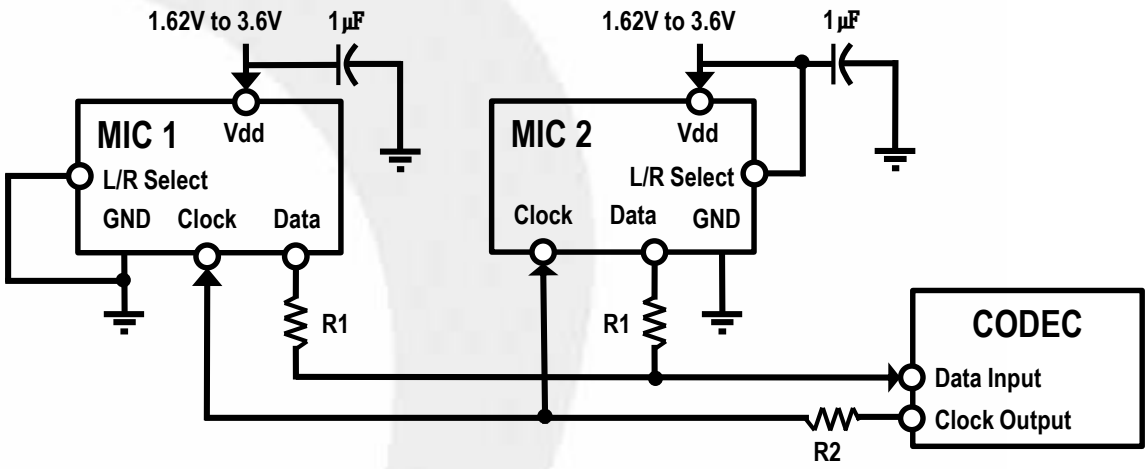
7. MEASUREMENT CIRCUIT



8. PIN DESCRIPTION

Pin Name	Description
Vdd	Supply and IO voltage for the microphone
L/R Select	Left/Right (DATA2 / DATA1) Channel selection
CLOCK	Clock input to the microphone
DATA	PDM data output from the microphone
GND	Ground

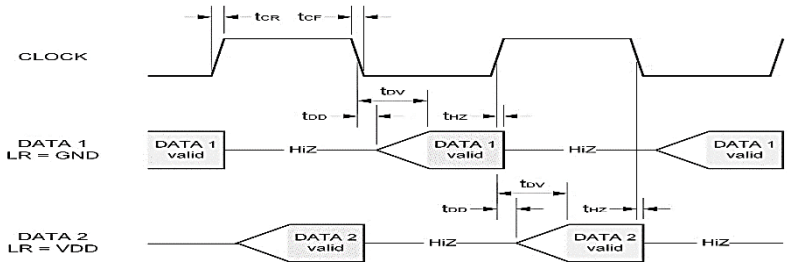
9. INTERFACE CIRCUIT & CHANNEL DATA CONFIGURATION



Data symbol in interface timing chart	L/R Select connected to	Data asserted at	Data sampled at
DATA1 [MIC1(Low)]	GND	Falling clock edge	Rising clock edge
DATA2 [MIC2(High)]	Vdd	Rising clock edge	Falling clock edge

Note 1 : Stereo operation is accomplished by connecting the L/R Sel. pin either to Vdd or GND on the phone PWB. Bypass Capacitors near each MIC. on Vdd are recommended to provide maximum SNR performance.
Note 2 : R1(Data source termination Resister) should be as close as possible to each the MIC. (50Ω~100Ω)
Note 3 : R2(Clock source termination Resister) should be as close as possible to the CODEC. (50Ω~100Ω)

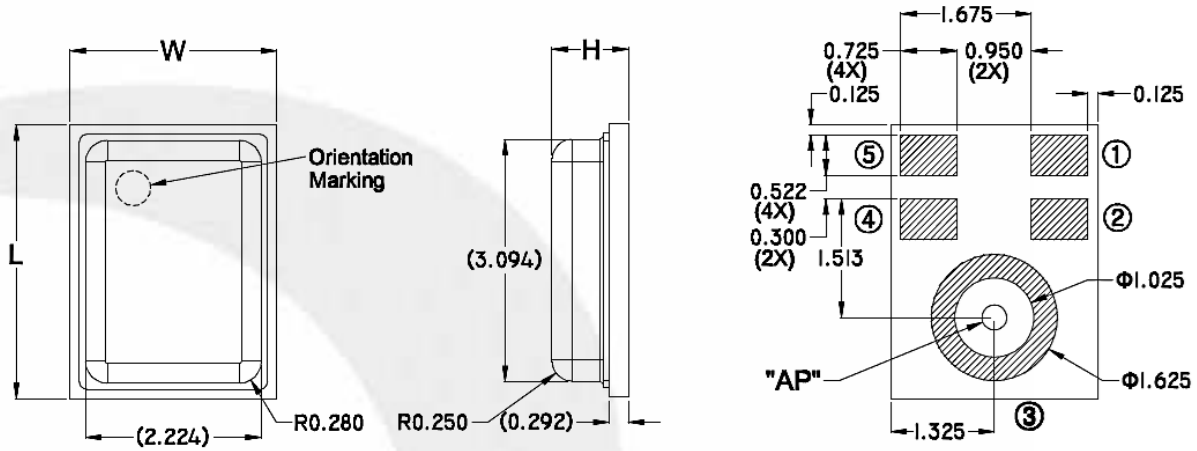
10. INTERFACE TIMING CHART



With defining a minimum value for t_{DD} and a maximum value for t_{HZ} it is secured that the driven DATA signals of the right and the left channel don't overlap.
A definition of a maximum value for t_{DD} is not necessary, instead t_{DV} defines the time until the driven DATA is valid.

11. MECHANICAL CHARACTERISTICS

Dimensions (Unit : mm)



TOP VIEW SIDE VIEW BOTTOM VIEW

Pin #	Pin Name	Type	Description
1	DATA	Digital O	PDM data output
2	L/R	L/R Select	Left/Right channel selection
3	GND	Ground	Ground
4	CLK	Clock	Clock input
5	VDD	Power	Supply and I/O voltage

Note : All ground Pins must be connected to ground.
"3"Pin must be sealed by solder paste on the PWB.
General Tolerance ±0.08mm.