DATASHEET

BoT-nLE521

DATASHEET

CONFIDENTEAL INFORMATION

V1.2.1

chipsen

List of Contents

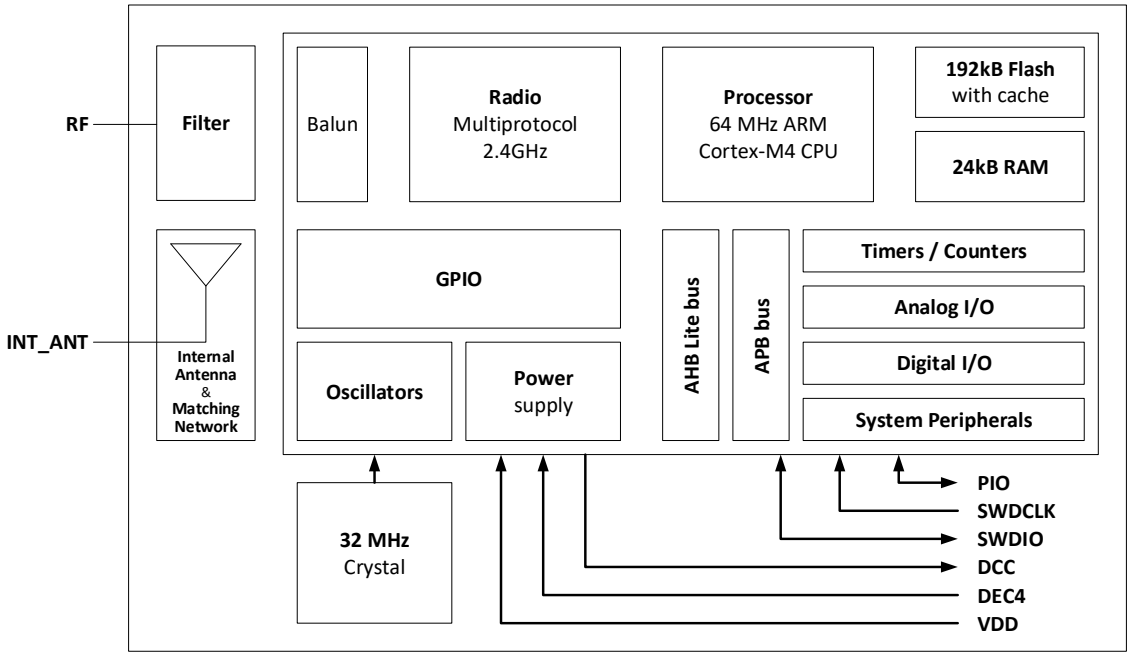
1. General

1.1 Overview

The BoT-nLE521 module is a cost-effective, low-power, true system-on-chip (SoC) for Bluetooth Smart (Bluetooth low energy) applications. It enables robust BLE slave nodes to be built with very low total bill-of-material costs. BoT-nLE521 combines an excellent RF transceiver with an industry-standard enhanced Cortec-M4 CPU, in-system programmable flash memory, 24kB RAM, and many other powerful supporting features and peripherals. The BoT-nLE521 is suitable for systems where very low power

Consumption is required. Very low-power sleep modes are available. Short transition times between operating modes further enable low power consumption.

1.2 Block Diagram



BoT-nLE521 Block Diagram

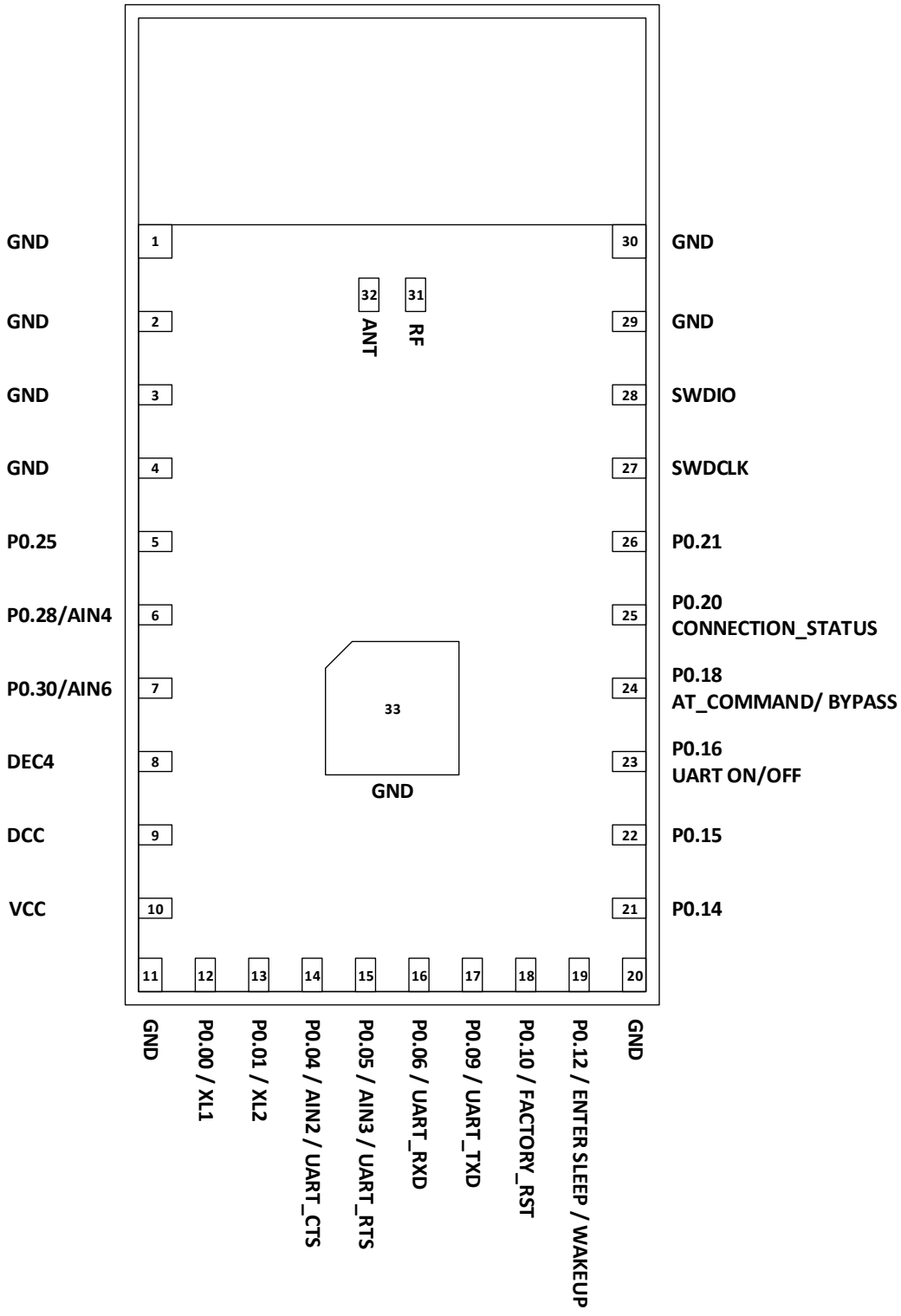
1.3 Features

- BT Ver. : Bluetooth 5
- Built in Antenna Bluetooth Smart (Bluetooth Low Energy) Module.
- ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz
- Memory: 192 kB Flash / 24 kB RAM
- RF Output Power: MAX +4 dBm (-20 ~ 4 dBm)
- RF Receive Sensitivity: -96 dBm
- Type 2 near field communication (NFC-A) tag with wakeup-on-field and touch to-pair capabilities
- Fully automatic LDO and DC/DC regulator system (Used LDO by Default)
- Temperature Sensor
- UART (CTS/RTS) with EasyDMA, SPI, and I2C data interfaces.
- 12-Bit 200 ksps ADC with - 8 configurable channels with programmable gain
- Size: 15 mm x 8 mm x 1.8 mm
- Operating Voltage: 1.7V to 3.6V
- Operating Temperature: -40 to +85℃
- RoHS compliant

1.4 Application

- Computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- Interactive entertainment devices
- Remote control
  - Gaming controller
- Beacons
- Personal Area Networks
  - Health/fitness sensor and monitor devices
  - Medical devices
  - Key-fobs + wrist watches
- Remote control toys

1.5 Pin Configuration

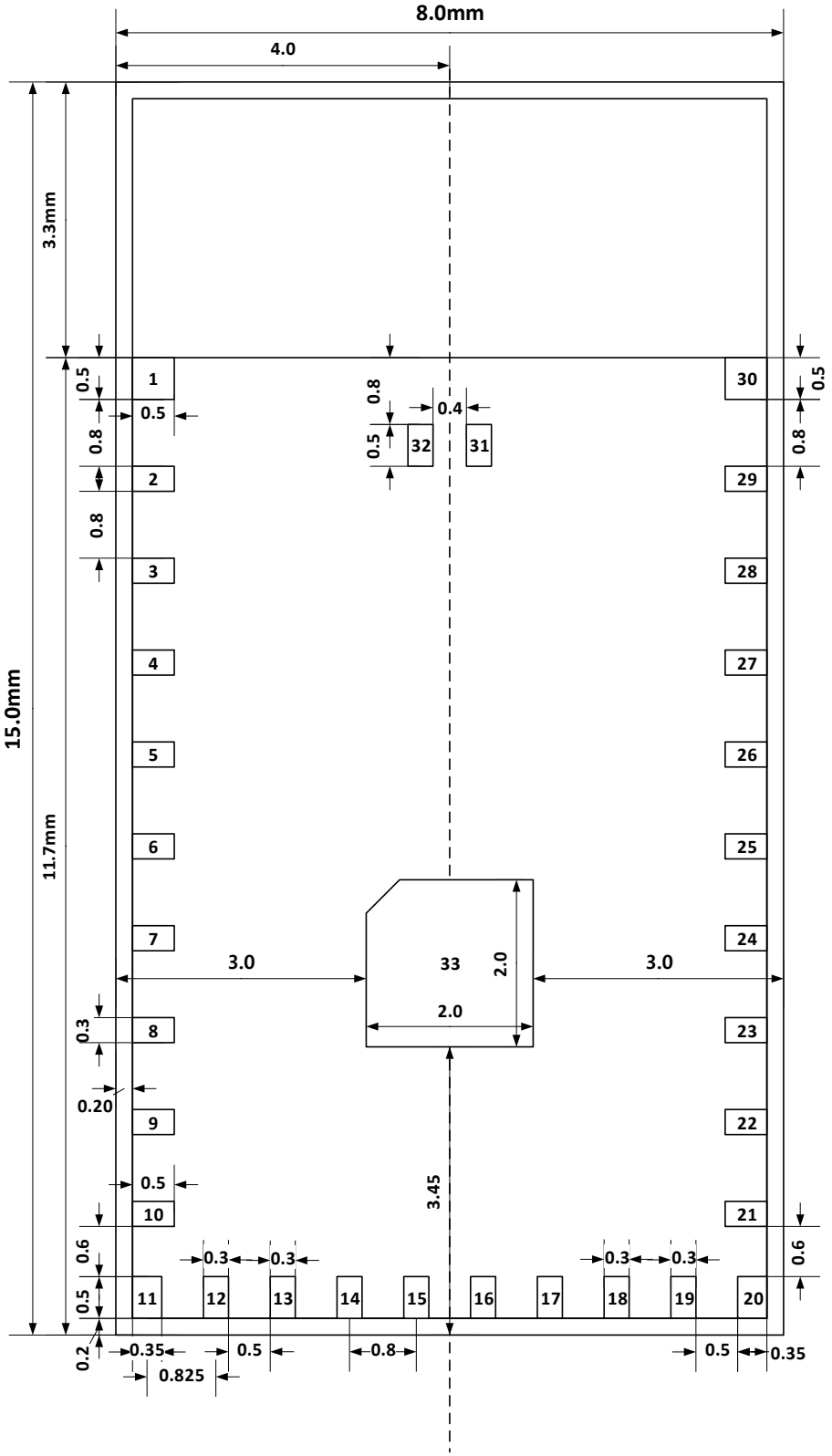


TOP VIEW

1.6 PIN Description

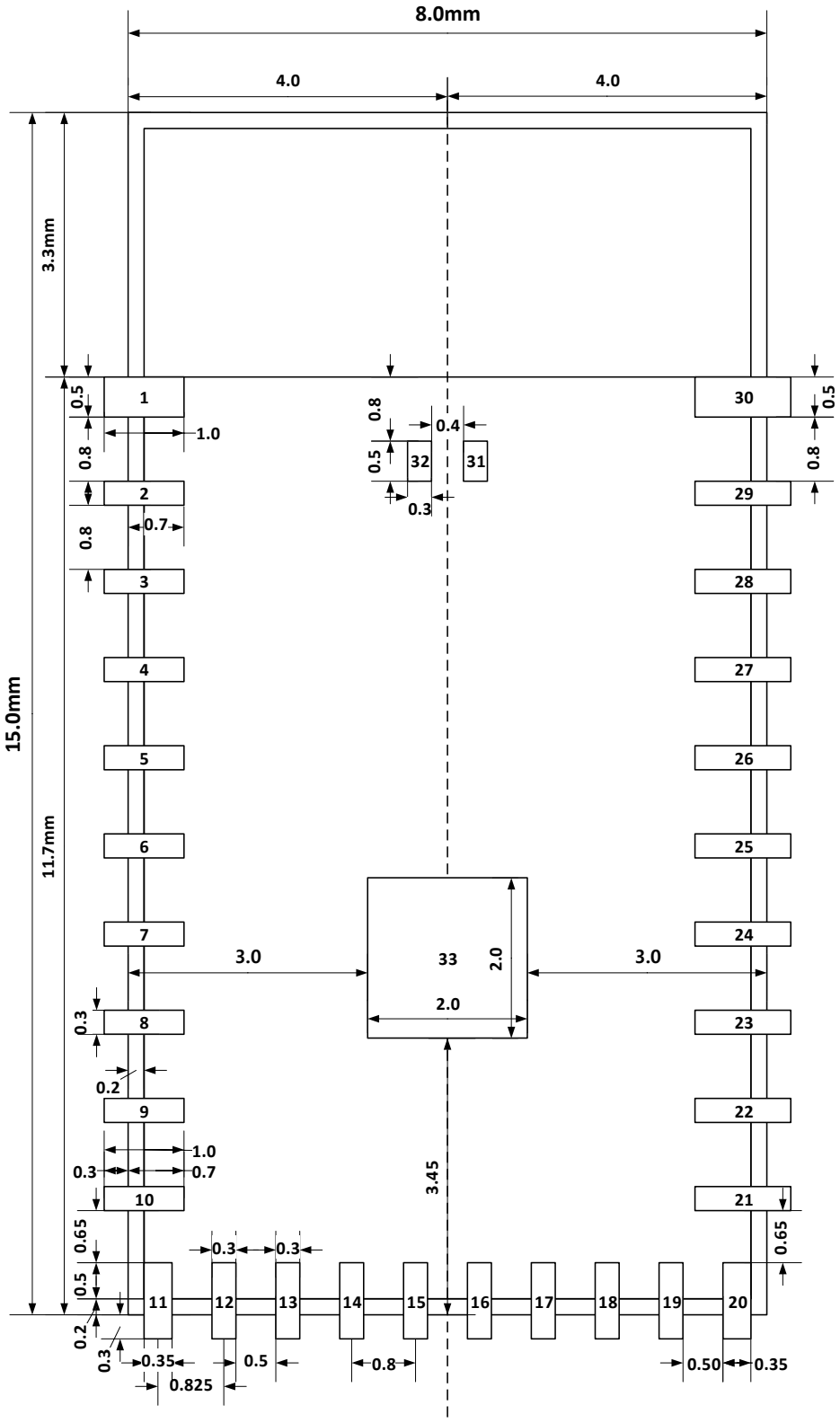
Pin No.	Pin Name	Pin Function	Description
01	GND	GROUND	Ground Pin.
02	GND	GROUND	Ground Pin.
03	GND	GROUND	Ground Pin.
04	GND	GROUND	Ground Pin.
05	P0.25	DIGITAL I/O	General purpose I/O pin.
06	P0.28	DIGITAL I/O	General purpose I/O pin.
	AIN4	ANALOG INPUT	SAADC/COMP input
07	P0.30	DIGITAL I/O	General purpose I/O pin.
	AIN6	ANALOG INPUT	COMP input
08	DEC4	POWER	1.3 V regulator supply decoupling Input from DC/DC converter. Output from 1.3 V LDO
09	DCC	POWER	DC/DC regulator output
10	VCC	POWER	Power supply pin.
11	GND	GROUND	Ground Pin.
12	P0.00	DIGITAL I/O	General purpose I/O pin.
	XL1	ANALOG INPUT	Connection for 32.768 kHz crystal (LFXO)
13	P0.01	DIGITAL I/O	General purpose I/O pin.
	XL2	ANALOG INPUT	Connection for 32.768 kHz crystal (LFXO)
14	P0.04	DIGITAL I/O	General purpose I/O pin.
	AIN2	ANALOG INPUT	SAADC/COMP input
	CTS	DIGITAL OUTPUT	UART CTS
15	P0.05	DIGITAL I/O	General purpose I/O pin.
	AIN3	ANALOG INPUT	SAADC/COMP input
	RTS	DIGITAL INPUT	UART RTS
16	P0.06	DIGITAL I/O	General purpose I/O pin.
	RXD	DIGITAL INPUT	UART RXD
17	P0.09	DIGITAL I/O	General purpose I/O pin.
	TXD	DIGITAL OUTPUT	UART TXD
18	P0.10	DIGITAL I/O	General purpose I/O pin.
	FACTORY_RST	DIGITAL INPUT	DISCONNECT & FACTORY_RESET
19	P0.12	DIGITAL I/O	General purpose I/O pin.
	ENTER_SLEEP /WAKE_UP	DIGITAL INPUT	ENTER_SLEEP / WAKE_UP
20	GND	GROUND	Ground Pin.
21	P0.14	DIGITAL I/O	General purpose I/O pin.
22	P0.15	DIGITAL I/O	General purpose I/O pin.
23	P0.16	DIGITAL I/O	General purpose I/O pin.
	UART ON/OFF	DIGITAL INPUT	UART ENABLE / DISABLE
24	P0.18	DIGITAL I/O	General purpose I/O pin.
	AT COMMAND /BYPASS	DIGITAL INPUT	AT COMMAND/BYPASS
25	P0.20	DIGITAL I/O	General purpose I/O pin.
	CONNECTION STATUS	DIGITAL OUTPUT	CONNECTION STATUS
26	P0.21	DIGITAL I/O	General purpose I/O pin.
27	SWDCLK	DIGITAL INPUT	Serial Wire Debug clock input for debug and programming
28	SWDIO	DIGITAL I/O	Serial Wire Debug I/O for debug and programming
29	GND	GROUND	Ground Pin.
30	GND	GROUND	Ground Pin.
31	RF	RF IN / OUT PORT	Bluetooth 50Ω transmitter output / receiver input
32	ANT	INTERNAL ANTENNA IN / OUT	Internal antenna. It should be connected to Pin 32 RF for normal operation.
33	GND	GROUND	Ground Pin.

1.7 Dimensions



TOP VIEW

1.8 Land Pattern



Land Pattern (TOP VIEW)

2. Characteristics

2.1 Electrical Characteristics

▪ Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
VDD		-0.3	+3.9	V
GND			0	V
$V_{I/O}$, VDD≤3.6V		-0.3	VDD + 0.3	V
$V_{I/O}$, VDD >3.6V		-0.3	+3.9	V
Storage temperature		-40	+125	℃
Radio ra	RF Input Level		10	dBm
MSL	Moisture Sensitivity Level	2		
ESD HBM	Human Body Model		4	kV
ESD CDM	Charged Device Model		1000	V
Endurance	Flash Memory Endurance	10000		write/erase cycles
Retention	Flash Memory Retention	10 years		At 40 ℃

▪ Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD	LDO Regulator Operation (Default Mode)	1.7	3.0	3.6	V
VDD	DC/DC Regulator Oprtation	2.1	3.0	3.6	V
$t_{R_}$VDD	Supply rise time (0V to 1.7V)			60	ms
TA	Operation temperature	-40	25	85	℃

▪ DC Characteristics

Symbol	Parameter (condition)	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	0.7 X VDD		VDD	V
V_{IL}	Input low voltage	VSS		0.3 X VDD	V
$V_{OH,SD}$	Output high voltage, standard drive, 0.5 mA, VDD	VDD-0.4		VDD	V
$V_{OH,HDH}$	Output high voltage, high drive, 5 mA, VDD ≥ 2.7	VDD-0.4		VDD	V
$V_{OH,HDL}$	Output high voltage, high drive, 3 mA, VDD ≥ 1.7	VDD-0.4		VDD	V
$V_{OL,SD}$	Output low voltage, standard drive, 0.5 mA, VDD	VSS		VSS +0.4	V
$V_{OL,HDH}$	Output low voltage, high drive, 5 mA, VDD ≥ 2.7 V	VSS		VSS +0.4	V
$V_{OL,HDL}$	Output low voltage, high drive, 3 mA, VDD ≥ 1.7 V	VSS		VSS +0.4	V
R_{PU}	Pull-up resistance	11	13	16	kΩ
R_{PD}	Pull-down resistance	11	13	16	kΩ
I_{TX},+4dBm,DCDC	TX only run current (DCDC, 3V) P_{RF}=+4 dBm		7.0		mA
I_{TX},+4dBm	TX only run current P_{RF}=+4 dBm		15.4		mA
I_{RX},1M,DCDC	RX only run current (DCDC, 3V) 1Msps		4.6		mA
I_{RX},1M	RX only run current 1Msps		10.0		mA
I_{RX},2M,DCDC	RX only run current (DCDC, 3V) 2Msps		5.2		mA
I_{RX},2M	RX only run current 2Msps		11.2		mA
$I_{ON\_RAMOFF\_EVENT}$	System ON, No RAM retention, Wake on any event		0.6		µA
$I_{ON\_RAMON\_EVENT}$	System ON, Full 24 kB RAM retention, Wake on any event		0.8		µA
$I_{ON\_RAMON\_POF}$	System ON, Full 24 kB RAM retention, Wake on any event, Power fail comparator enabled		0.8		µA
$I_{ON\_RAMON\_GPIOTE}$	System ON, Full 24 kB RAM retention, Wake on GPIOTE input (Event mode)		3.3		µA
$I_{ON\_RAMON\_GPIOTEPORT}$	System ON, Full 24 kB RAM retention, Wake on GPIOTE PORT event		0.8		µA
$I_{ON\_RAMON\_RTC}$	System ON, Full 24 kB RAM retention, Wake on RTC (running from LFRC clock)		1.5		µA
$I_{OFF\_RAMOFF\_RESET}$	System OFF, No RAM retention, Wake on reset		0.3		µA
$I_{OFF\_RAMON\_RESET}$	System OFF, Full 24 kB RAM retention, Wake on reset		0.5		µA

2.2 RF Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
f_{OP}	Operating frequencies	2402		2480	MHz
$f_{PLL,PROG,RES}$	PLL programming resolution		2		kHz
$f_{PLL,CH,SP}$	PLL channel spacing		1		MHz
$f_{DELTA,BLE,1M}$	Frequency deviation @ BLE 1Msps		±250		kHz
$f_{DELTA,BLE,2M}$	Frequency deviation @ BLE 2Msps		±500		kHz
P_{RF}	Maximum output power		0	4	dBm
P_{RFC}	RF power control range		24		dB
P_{RFCR}	RF power accuracy			±4	dB
$P_{RF1.1}$	1st Adjacent Channel Transmit Power 1 MHz (1		-25		dBc
$P_{RF2.1}$	2nd Adjacent Channel Transmit Power 2 MHz (1		-50		dBc
$P_{RF1.2}$	1st Adjacent Channel Transmit Power 2 MHz (2		-25		dBc
$P_{RF2.2}$	2nd Adjacent Channel Transmit Power 4 MHz (2		-50		dBc
$P_{RX,MAX}$	Maximum received signal strength at < 0.1% PER		0		dBm
$P_{SENS,IT,SP,1M,BLE}$	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER=1E-3		-96		dBm
$P_{SENS,IT,SP,2M,BLE}$	Sensitivity, 2Msps BLE ideal transmitter, <=37		-93		dBm
$RSSI_{ACC}$	RSSI Accuracy Valid range -90 to -20 dBm		±2		dB
$RSSI_{RESOLUTION}$	RSSI resolution		1		dB
$RSSI_{PERIOD}$	Sample period		8		us

2.3 Reference RF Measurement Report (Radiation)

9 RF test cases started: Tue Sep 3 10:42:48 2019
_____Output Power (TP/TRM-LE/CA/BV-01-C)
Initial conditions:

Test Method:	Test mode
Hopping:	off
Payload:	PRBS9
Payload's length:	37 bytes
Number of packets:	1
Path losses:	21.00dB

Limits:
-20.00dBm <= Pavg <= 10.00dBm, Ppk-av <= 3.00dB
Results (power in dBm):

#ch	f(MHz)	Pavg	Ppk	Ppk-av	Pmin	Verdict
0	2402	-1.56	-1.29	0.27	-1.89	PASSED
19	2440	-0.49	-0.29	0.20	-0.78	PASSED
39	2480	-0.81	-0.56	0.25	-1.12	PASSED

Test time: 1 sec.
_____In-band emissions (TP/TRM-LE/CA/BV-03-C)
Initial conditions:

Test Method:	Test mode

Payload:	PRBS9
Payload's length:	37 bytes
Number of sweeps:	10
Path losses:	21.00dB

Limits:

P[N]<=-20.00dBm if abs(M-N)=2,P[N]<=-30.00dBm if abs(M-N)>3,-30.00dBm<=P[i]<=-20.00dBm less then for 3 channels

Results:

freq=2406MHz (M=4), P[N] in dBm:

N	P[N]	N	P[N]	N	P[N]	N	P[N]
2401	-39.73	2422	-40.51	2443	-40.23	2464	-39.96
2402	-40.02	2423	-40.16	2444	-39.62	2465	-39.98
2403	-40.03	2424	-44.48	2445	-39.84	2466	-40.07
2404	-33.09	2425	-44.41	2446	-40.06	2467	-39.98
2405	-23.96	2426	-44.41	2447	-39.91	2468	-39.97
2406	-2.25	2427	-39.90	2448	-39.94	2469	-40.09
2407	-21.33	2428	-40.10	2449	-39.62	2470	-40.06
2408	-33.25	2429	-40.10	2450	-39.78	2471	-39.78
2409	-40.29	2430	-40.14	2451	-40.18	2472	-39.80
2410	-40.03	2431	-40.23	2452	-39.80	2473	-40.22
2411	-40.20	2432	-40.15	2453	-39.90	2474	-39.96
2412	-40.14	2433	-39.92	2454	-39.97	2475	-39.64
2413	-40.17	2434	-39.98	2455	-39.87	2476	-39.97
2414	-40.20	2435	-40.07	2456	-39.79	2477	-39.87
2415	-40.32	2436	-40.02	2457	-40.03	2478	-39.87
2416	-39.95	2437	-39.78	2458	-39.92	2479	-40.06
2417	-39.93	2438	-40.03	2459	-40.09	2480	-40.07
2418	-40.00	2439	-40.27	2460	-39.91	2481	-39.89
2419	-40.08	2440	-39.95	2461	-39.83		
2420	-40.12	2441	-40.27	2462	-39.64		
2421	-40.21	2442	-39.97	2463	-40.14		

Verdict: PASSED

freq=2440MHz (M=38), P[N] in dBm:

N	P[N]	N	P[N]	N	P[N]	N	P[N]
2401	-39.81	2422	-40.25	2443	-39.74	2464	-40.00
2402	-40.22	2423	-40.09	2444	-39.99	2465	-40.18
2403	-40.24	2424	-40.08	2445	-39.77	2466	-40.05
2404	-40.31	2425	-39.75	2446	-39.97	2467	-39.51
2405	-39.94	2426	-39.94	2447	-39.94	2468	-40.11
2406	-39.97	2427	-39.91	2448	-39.83	2469	-39.93
2407	-40.12	2428	-40.17	2449	-39.84	2470	-40.07
2408	-40.31	2429	-40.00	2450	-39.78	2471	-39.89
2409	-40.05	2430	-39.90	2451	-39.82	2472	-39.81
2410	-40.47	2431	-40.05	2452	-39.90	2473	-40.00
2411	-40.09	2432	-40.00	2453	-40.13	2474	-39.92
2412	-39.92	2433	-40.31	2454	-39.67	2475	-39.96
2413	-40.09	2434	-40.06	2455	-39.94	2476	-39.96
2414	-39.86	2435	-40.18	2456	-39.93	2477	-40.03
2415	-39.99	2436	-40.19	2457	-39.91	2478	-40.27
2416	-40.11	2437	-40.16	2458	-44.38	2479	-40.10
2417	-40.44	2438	-32.25	2459	-44.24	2480	-39.91
2418	-42.71	2439	-22.75	2460	-44.12	2481	-39.93
2419	-44.08	2440	-0.98	2461	-39.71		
2420	-42.68	2441	-20.11	2462	-39.62		
2421	-40.30	2442	-32.48	2463	-40.29		

Verdict: PASSED

freq=2476MHz (M=74), P[N] in dBm:

N	P[N]	N	P[N]	N	P[N]	N	P[N]
2401	-40.21	2422	-40.12	2443	-40.20	2464	-39.95
2402	-40.36	2423	-40.21	2444	-39.72	2465	-39.98
2403	-40.12	2424	-40.27	2445	-39.80	2466	-39.97
2404	-40.12	2425	-40.13	2446	-39.89	2467	-39.94
2405	-40.07	2426	-40.13	2447	-40.08	2468	-39.77

2406	-40.03	2427	-39.95	2448	-39.71	2469	-39.80
2407	-40.15	2428	-40.07	2449	-39.98	2470	-39.86
2408	-40.20	2429	-39.91	2450	-39.62	2471	-40.38
2409	-40.28	2430	-40.10	2451	-40.06	2472	-39.85
2410	-40.05	2431	-40.18	2452	-39.96	2473	-39.89
2411	-40.09	2432	-40.38	2453	-40.02	2474	-32.81
2412	-39.97	2433	-39.92	2454	-42.39	2475	-23.52
2413	-40.22	2434	-39.95	2455	-43.75	2476	-1.96
2414	-40.02	2435	-40.29	2456	-42.48	2477	-20.49
2415	-40.49	2436	-40.17	2457	-39.68	2478	-32.82
2416	-40.27	2437	-40.14	2458	-40.01	2479	-39.55
2417	-39.98	2438	-40.22	2459	-39.72	2480	-39.90
2418	-39.85	2439	-39.94	2460	-39.81	2481	-40.05
2419	-40.03	2440	-40.18	2461	-40.13		
2420	-40.09	2441	-39.97	2462	-39.69		
2421	-40.39	2442	-39.86	2463	-40.04		

Verdict: PASSED

Test time: 3 min. 5 sec.

_____Modulation Characteristics (TP/TRM-LE/CA/BV-05-C)

Initial conditions:

Test Method:	Test mode
Hopping:	off
Payload:	11110000 and 1010 bit patterns
Payload's length:	37 bytes
Number of packets:	10

Limits:

225.0KHz <= df1_avg <= 275.0KHz, df2_pass_rate >= 99.90%, df2/df1 >= 0.80

Results (frequency deviations in KHz):

#ch	f(MHz)	df1_avg	df2_avg	df2_min	df2_rate(%)	df2/df1	Verdict	
0	2402	258.8	253.2	223.6	100.00		0.98	PASSED
19	2440	258.0	256.4	230.5	100.00		0.99	PASSED
39	2480	257.6	257.1	231.6	100.00		1.00	PASSED

Test time: 3 sec.

_____Carrier frequency offset and drift (TP/TRM-LE/CA/BV-06-C)

Initial conditions:

Test Method:	Test mode
Payload:	1010 bit pattern
Payload's length:	37 bytes
Number of packets:	10

Limits:

|fTX-f[n]| <= 150.0KHz, |f[0]-f[n]| <= 50.0KHz, |f[1]-f[0]| <= 23.0KHz, |f[n]-f[n-5]| <= 20.0KHz

Results (maximum of absolute values in KHz):

#ch	f(MHz)	fTX-f[n]	f[0]-f[n]	f[1]-f[0]	f[n]-f[n-5]	Verdict	
0	2402	12.1	-5.4	-3.7	3.8		PASSED
19	2440	12.4	-4.2	1.7	-4.7		PASSED
39	2480	12.8	-5.0	-3.0	-3.3		PASSED

Test time:<1 sec.

_____Receiver sensitivity (TP/RCV-LE/CA/BV-01-C)

Initial conditions:

Test Method:	Test mode	
Payload:	PRBS9	
Payload's length:	37 bytes	
Packets to transmit:	1500	
RX (DUT) power:		-70.00dBm
Path losses:	21.00dB	
Dirty TX mode:		On
PER limit mode:		Specification

Limits:

pkts_sent >= 1500, PER < 30.80%

Results:

#ch	f(MHz)	pkts_sent	pkts_rcvd	PER(%)	Verdict	
0	2402	1500		1500	0.000	PASSED

19	2440	1500	1500	0.000	PASSED	
39	2480	1500	1500	0.000	PASSED	

Test time: 4 sec.

_____Maximum input signal level (TP/RCV-LE/CA/BV-06-C)

Initial conditions:

Test Method:	Test mode
Payload:	PRBS9
Payload's length:	37 bytes
Packets to transmit:	1500
RX (DUT) power:	-30.00dBm
Path losses:	21.00dB
PER limit mode:	Specification

Limits:

pkts_sent >= 1500, PER < 30.80%

Results:

#ch	f(MHz)	pkts_sent	pkts_rcvd	PER(%)	Verdict		
0	2402	1500	1500	0.000	PASSED		
19	2440	1500	1500	0.000	PASSED		
39	2480	1500	1500	0.000	PASSED		

Test time: 3 sec.

_____PER Report Integrity (TP/RCV-LE/CA/BV-07-C)

Initial conditions:

Test Method:	Test mode
Payload:	PRBS9
Payload's length:	37 bytes
Packets to transmit:	1500
RX (DUT) power:	-30.00dBm
Path losses:	21.00dB
PER limit mode:	Specification

Limits:

pkts_sent >= 1500, 50.00% <= PER <= 65.40%

Results:

#ch	f(MHz)	pkts_sent	pkts_rcvd	PER(%)	Verdict		
0	2402	1500	750	50.000	PASSED		
19	2440	1500	750	50.000	PASSED		
39	2480	1500	750	50.000	PASSED		

Test time: 3 sec.

_____Quick (Output Power + Modulation Characteristics + Carrier Frequency Offset Drift)

Initial conditions:

Test Method:	Test mode
Hopping:	off
Payload:	11110000 and 1010 bit patterns
Payload's length:	37 bytes
Number of packets:	2
Path losses:	21.00dB

Limits:

-20.00dBm < Pavg < 10.00dBm, Ppk-av < 3.00dB

df0_max <= 150.0 KHz, df0_min >= -150.0 KHz

|fTX-f[n]| <= 150.0KHz, |f[0]-f[n]| <= 50.0KHz, |f[1]-f[0]| <= 23.0KHz, |f[n]-f[n-5]| <= 20.0KHz

225.0KHz <= df1_avg <= 275.0KHz, df2_pass_rate >= 99.90%, df2/df1 >= 0.80

Results (power in dBm, frequency offsets in KHz):

#ch	f(MHz)	Pavg	Ppk	Ppk-av	Pmin	df0_max	df0_min
0	2402	-2.14	-1.35	0.79	-3.16	10.5	8.8
19	2440	-0.76	0.04	0.80	-1.77	10.0	8.9
39	2480	-1.04	-0.30	0.74	-2.04	12.7	12.1

Results (maximum of absolute values in KHz):

#ch	f(MHz)	fTX-f[n]	f[0]-f[n]	f[1]-f[0]	f[n]-f[n-5]
0	2402	12.3	-3.3	2.3	-3.8
19	2440	12.0	3.1	-1.0	3.7
39	2480	12.1	-4.4	-4.1	2.7

Results (frequency deviations in KHz):

#ch	f(MHz)	df1_avg	df2_avg	df2_min	df2_rate(%)	df2/df1	Verdict

0	2402	258.4	253.7	229.1	100.00	0.98	PASSED
19	2440	258.3	256.9	233.6	100.00	0.99	PASSED
39	2480	258.1	256.4	229.1	100.00	0.99	PASSED

Test time: 2 sec.

_____Carr freq offset + Mod char (preamble)

Initial conditions:

Test Method:	Test mode
Hopping:	off
Payload's length:	37 bytes
Number of packets:	2

Limits:

df0_max <= 150.0 KHz, df0_min >= -150.0 KHz
df2_avg >= 185.0KHz, df2_min >= 92.5KHZ

Results (frequency offsets and deviations in KHz):

#ch	f(MHz)	df0_max	df0_min	df0_avg	df2_avg	df2_min	Verdict
0	2402	10.0	7.7	8.8	250.1	241.3	PASSED
19	2440	10.4	7.8	9.1	255.8	242.6	PASSED
39	2480	11.3	10.9	11.1	250.7	241.1	PASSED

Test time: 1 sec.

9 RF test cases completed: Tue Sep 3 10:46:11 2019

Total test time: 3 min. 23 sec.

3. Terminal Description

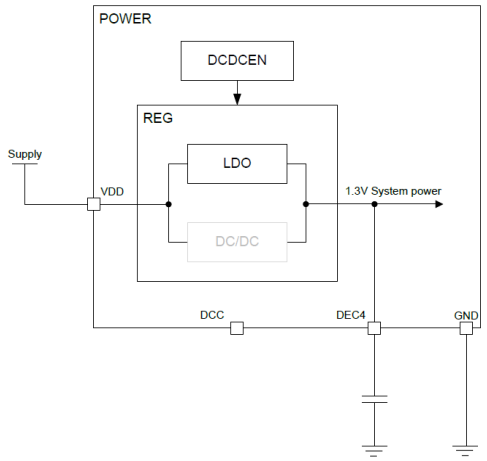
3.1 Regulator

The following internal power regulator alternatives are supported:

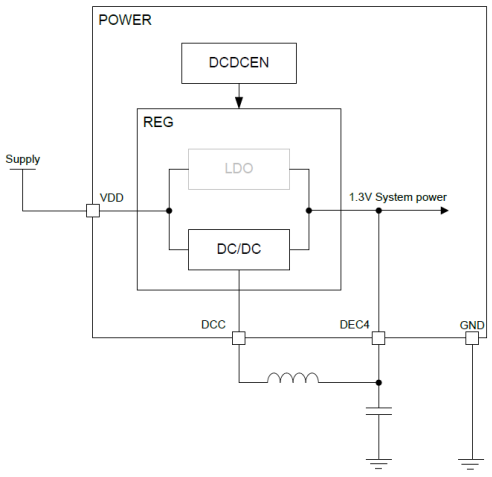
- Internal LDO regulator
- Internal DC/DC regulator

The LDO is the default regulator.

Using the DC/DC regulator will reduce current consumption compared to when using the LDO regulator, but the DC/DC regulator requires an external LC filter to be connected, as shown in Figure.



LDO Regulator Setup



DC/DC Regulator Setup

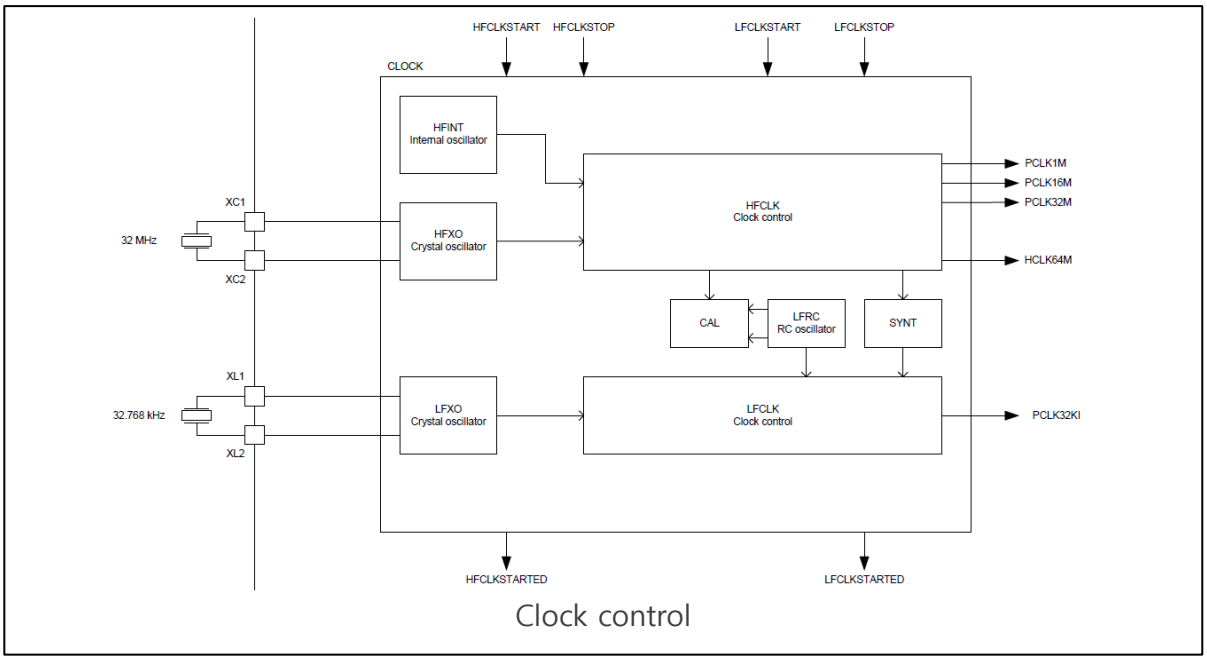
3.2 32.768KHz Crystal Oscillator

The BoT-nLE521 external 32.768KHz Crystal does not required for BLE mode

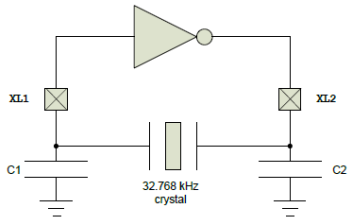
If you choose to use an internal 32.768kHz oscillator, an average of 10uA of current is consumed compared to an external crystal.

The ANT specification requires ± 50ppm accuracy for a 32.768kHz clock. The internal 32.768kHz oscillator may not meet specifications.

BoT-nLE521 F/W does not yet support ANT Mode.



Clock control



Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$
$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. Cpcb1 and Cpcb2 are stray capacitances on the PCB.

▪ 32.768 kHz RC oscillator (LFRC)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_LFRC}	Nominal frequency		32.768		kHz
f_{TOL_LFRC}	Frequency tolerance		±2		%
$f_{TOL\_CAL\_LFRC}$	Frequency tolerance for LFRC after calibration		±500		ppm

▪ 32.768 kHz crystal oscillator (LFXO)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_LFXO}	Crystal frequency		32.768		kHz
$f_{TOL\_LFXO\_BLE}$	Frequency tolerance requirement for BLE stack		±250		ppm
$f_{TOL\_LFXO\_ANT}$	Frequency tolerance requirement for ANT stack		±50		ppm
C_{L_LFXO}	Load capacitance			12.5	pF
C_{0_LFXO}	Shunt capacitance			2	pF
R_{S_LFXO}	Equivalent series resistance			100	kohm
P_{D_LFXO}	Drive level			1	uW
C_{pin}	Input capacitance on XL1 and XL2 pads		4		pF

4. Power Consumption

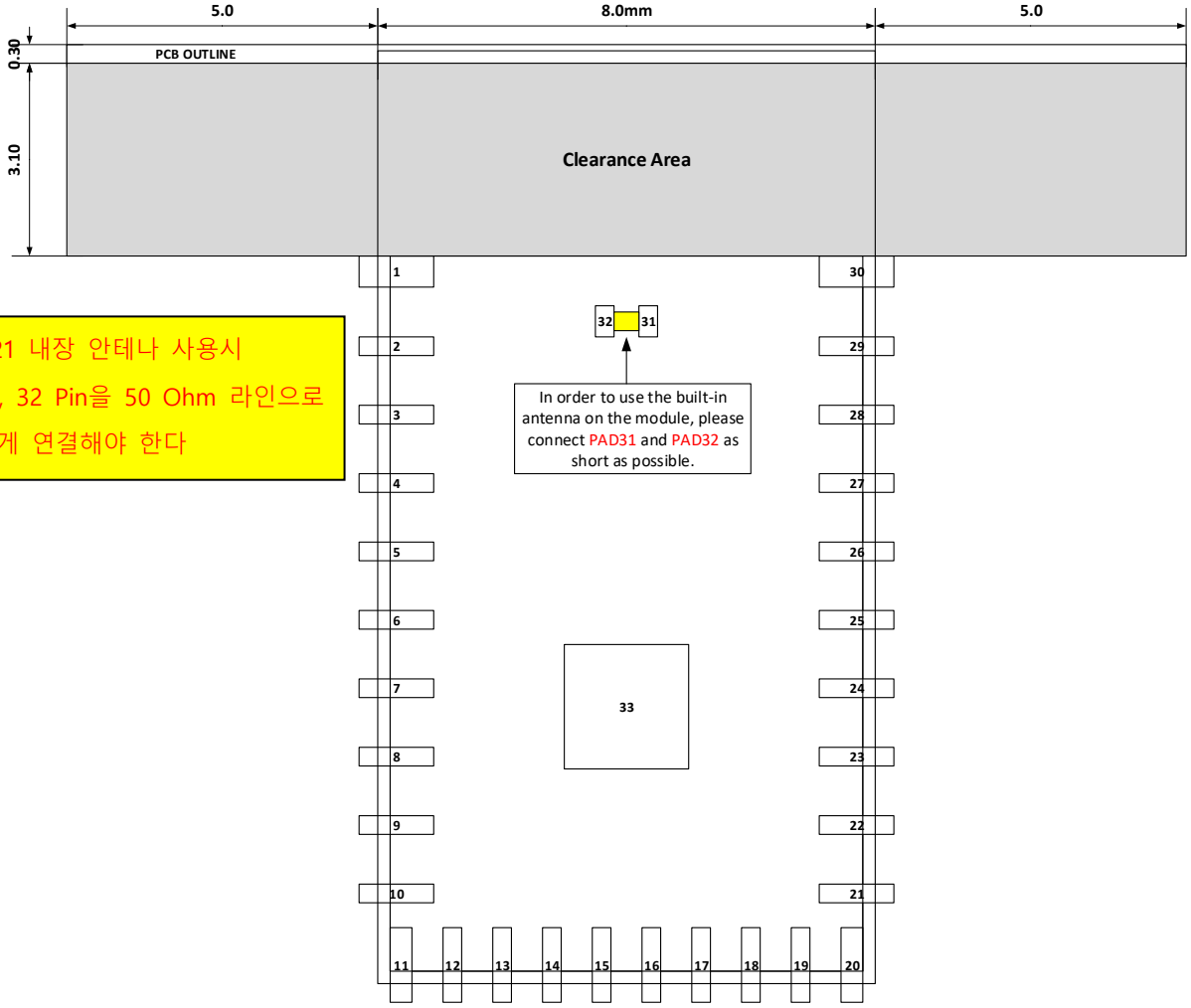
UART State / BoT State	UART ON(uA)	UART OFF(uA)		
		Internal Pull-Down	External Pull-Down 470K **Make internal pull-x register to no-pull state using "AT+INTPULLDOWN=OFF" command	Internal Pull-Down & External Pull-Down 470K
Advertising	592	255	23	256
Connected	839	524	296	532
Sleep	N/A	237	7	244

**measure condition Firmware version : over V0..8.0

Advertising interval : 1280ms

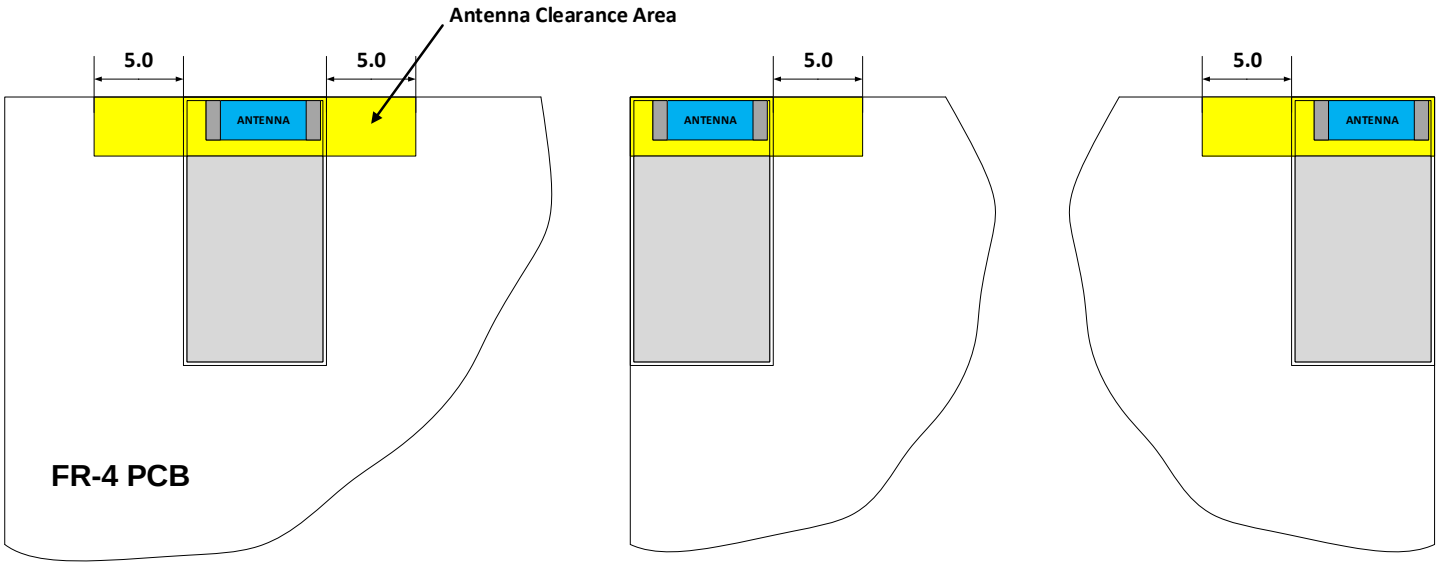
5. Antenna

5.1 Antenna Layout Guide

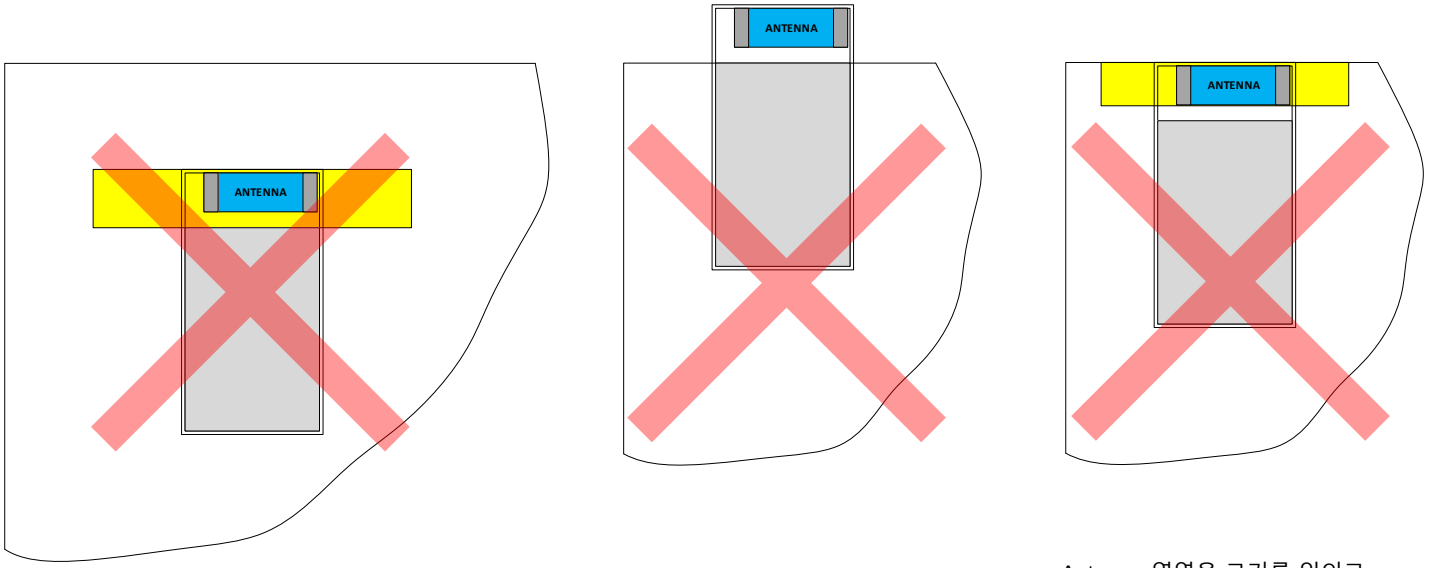


BoT-nLE521 내장 안테나 사용시
반드시 31, 32 Pin을 50 Ohm 라인으로
최대한 짧게 연결해야 한다

5.2 Recommended Module Mounting



Recommended Module Mounting Example



Antenna 영역을 GND가 둘러싸고 있는 형태

Antenna 영역이 PCB 외부에 장착된 형태

Antenna 영역을 크기를 임의로 조정 또는 Antenna 영역에 GND가 겹치는 형태

Wrong Module Mounting Example

6. Reflow Temperature Profiles

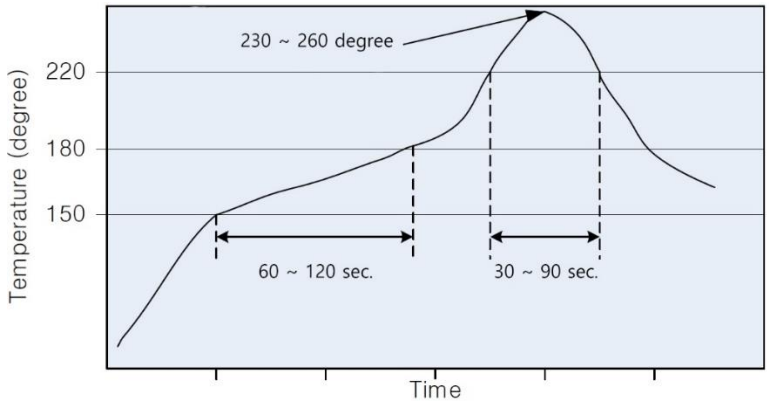
Recommended solder reflow profile are shown in below and follow the lead-free profile I accordance with JEDEC Std 20C.

Table lists the critical reflow temperatures.

Flux residue remaining from board assembly can contribute to electrochemical migration over time.

This depends on number of factors, including flux type, amount of flux residue remaining after reflow, and stress conditions during product use, such as temperature, humidity, and potential difference between pins.

Care should be taken in selecting production board/module assembly processes and materials, taking into account these factors.



Process Step	Lead-Free Solder
Ramp rate	3°C/sec
Preheat	Max. 150°C to 180°C, 60 to 180 sec
Time above liquidus	+220°C 30 to 90 sec
Peak temperature	+255°C ±5°C
Time within 5°C of peak temperature	10 to 20 sec
Ramp-down rate	6°C/sec max

WARNING : For BoT-nLE521

If you have reflow process multiple times in your product, you must be proceed this module in the final reflow process. If not the Shield can will drop out if shield-can adopted .

7. Application Schematic

7.1 Reference Application

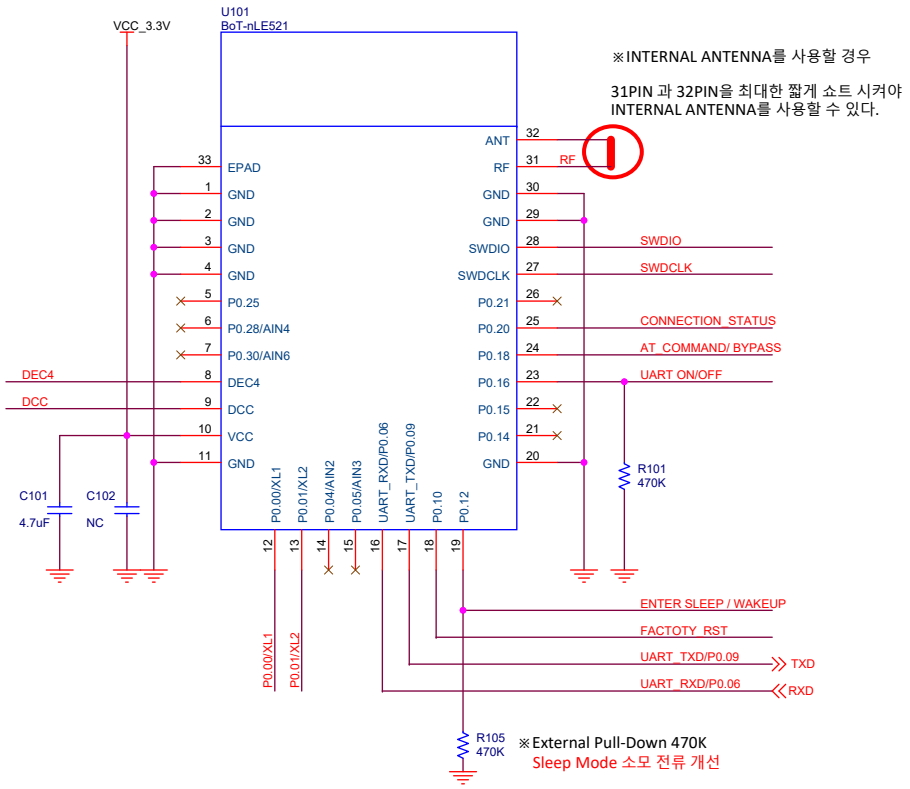
7.2 Internal ANT. / 3.3V UART Application

7.3 Internal ANT. / 5V UART Application

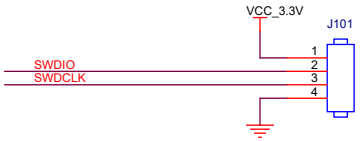
7.4 External ANT. / 3.3V UART Application

- All reference applications are attached next page.

▣ BoT-nLE521 REF. APPLICATION



J-LINK DEBUG PORT



※ Wireless Certification

무선 인증 진행 시 DTM F/W Download Port

ENTER SLEEP /WAKEUP
UART ON/OFF

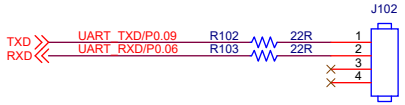
※펌웨어 V0.8.0 이상에서 유효한 기능임

INPUT	ENTER SLEEP / WAKEUP	UART ON /OFF
HIGH(RISING EDGE)	LOW POWER MODE	UART DISABLE
LOW(FALLING EDGE)	WAKE UP & REBOOTING	UART ENABLE

※ENTER SLEEP / WAKE UP
High Level(Rising Edge) 이 감지되면 저전력 모드로 진입이 되며,
저전력 모드상태에서는 Low Level (Falling Edge) 이 감지되면
Wake Up 되고 모듈이 자동으로 재부팅한다.

※UART ON / OFF
High Level(Rising Edge) 이 감지되면 UART가 동작을 멈추고(DISABLE)
저전력 모드로 진입
UART DISABLE 상태에서 Low Level (Falling Edge) 이 감지되면 UART 동작이
재시작(ENABLE)함.

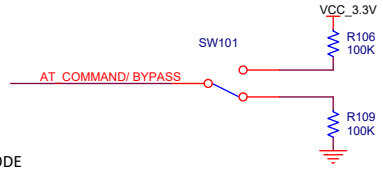
UART PORT



※UART Port for SIG / Wireless Certification

무선 인증 진행 시 DTM F/W로 주파수 컨트롤 시 UART를 사용
반드시 라인 절체할 수 있는 저항 필수 추가

AT_COMMAND/ BYPASS



■ UART MODE

INPUT	DESCRIPTION
HIGH	AT COMMAND MODE
LOW	BYPASS MODE (DATA MODE)

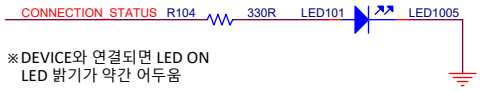
※DEVICE와 연결되기 전에는 AT COMMAND MODE로 동작
※DEVICE와 연결 후 UART MODE PIN HIGH,LOW로 UART MODE 동작 결정

CONNECTION_STATUS LED OPTION

■ CONNECTION STATE

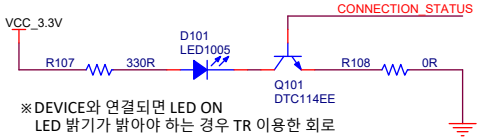
OUTPUT	DESCRIPTION
HIGH	DEVICE CONNECTION
LOW	DEVICE DISCONNECTION

■ EXAMPLE 1



※DEVICE와 연결되면 LED ON
LED 밝기가 약간 어두움

■ EXAMPLE 2



※DEVICE와 연결되면 LED ON
LED 밝기가 밝아야 하는 경우 TR 이용한 회로

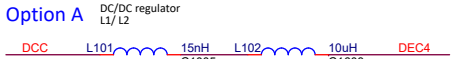
FACTOTY_RST

※FACTOTY_RST

DEFAULT SETTING은 INPUT 설정
4초 이상 HIGH 유지시 +OK 응답 후 공장초기화 상태로 복귀시킨다.

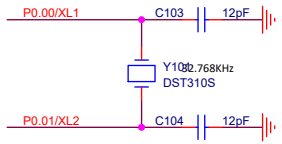
OPTION

Option A DC/DC regulator L1/ L2



DEFAULT LDO MODE, DO NOT DESIGN DC/DC MODE CIRCUIT

Option B



DEFAULT INTERNAL 32.768KHz MODE
DO NOT DESIGN EXTERNAL 32.768KHz CRYSTAL

※OPTION
DEFAULT F/W에서 OPTION A / B 지원하지 않음

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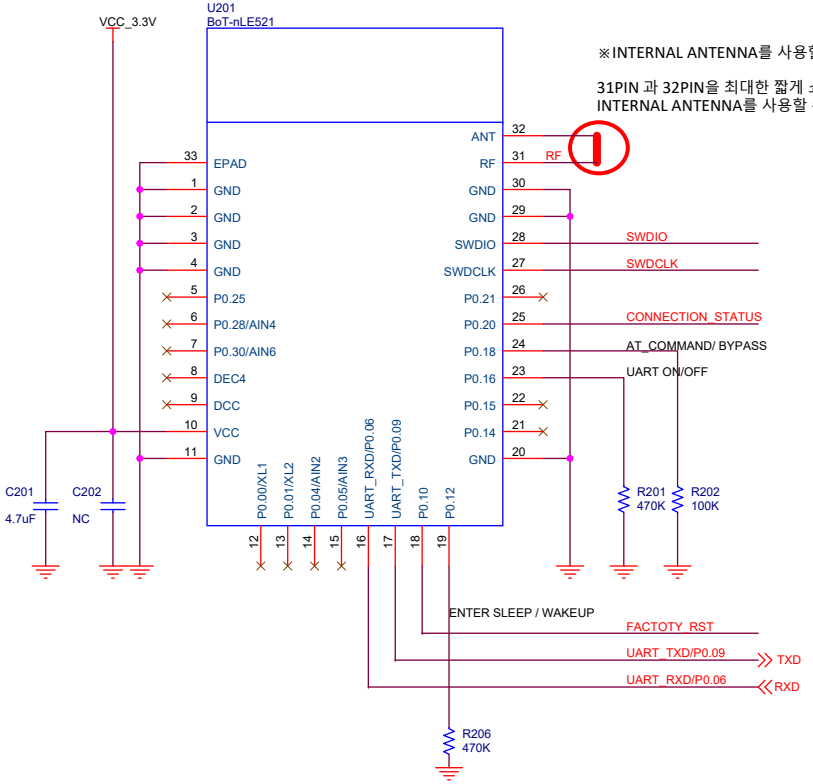
대 표 : 1599-6885
사 무 실 : 1599-6005

Title: BoT-nLE521 REF. APPLICATION
Size: A3 | Document Number: BoT-nLE521 REF. APPLICATION | Rev: 1.0
Date: Friday, October 11, 2019 | Sheet 1 of 4

▣ BoT-nLE521 REF. APPLICATION - UART 3.3V level input

■ Example Schematic

■ INTERNAL ANTENNA
■ UART 3.3V level input
■ Bypass in Bluetooth connected state
■ Default LDO Mode
■ Default Internal 32.768KHz Mode
■ UART ON
■ WAKE UP

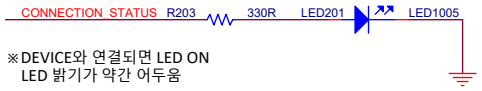


CONNECTION_STATUS LED OPTION

■ CONNECTION STATE

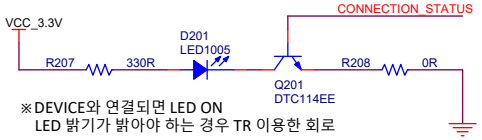
OUTPUT	DESCRIPTION
HIGH	DEVICE CONNECTION
LOW	DEVICE DISCONNECTION

■ EXAMPLE 1



※DEVICE와 연결되면 LED ON
LED 밝기가 약간 어두움

■ EXAMPLE 2



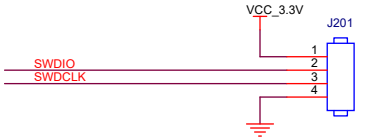
※DEVICE와 연결되면 LED ON
LED 밝기가 밝아야 하는 경우 TR 이용한 회로

FACTOTY_RST

※FACTOTY_RST

DEFAULT SETTING은 INPUT 설정
4초 이상 HIGH 유지시 +OK 응답 후 공장초기화 상태로 복귀시킨다.

J-LINK DEBUG PORT



※ Wireless Certification

무선 인증 진행 시 DTM F/W Download Port

ENTER SLEEP /WAKEUP

※ WAKE UP

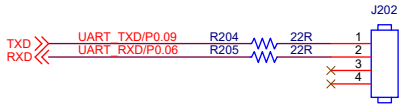
LOW INPUT : 저전력 모드로 들어가지 않고 동작상태

UART ON/OFF

※UART ON

LOW INPUT : UART ON (ENABLE) 상태

UART PORT



※UART Port for SIG / Wireless Certification

무선 인증 진행 시 DTM F/W로 주파수 컨트롤 시 UART를 사용
반드시 라인 절체할 수 있는 저항 필수 추가

AT_COMMAND/ BYPASS

■ BYPASS MODE

LOW INPUT : BYPASS MODE (DATA 전송 모드)

※DEVICE와 연결되기 전에는 AT COMMAND MODE로 동작

※DEVICE와 연결 후 UART MODE PIN HIGH,LOW로 UART MODE 동작 결정

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Title: BoT-nLE521 REF. APPLICATION

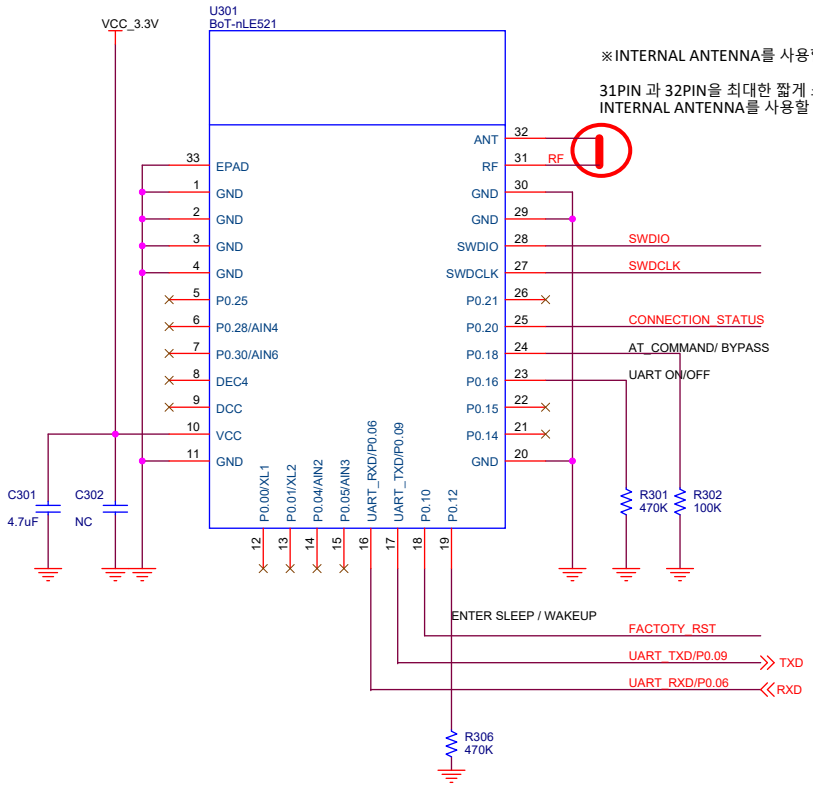
Size	Document Number	Rev
A3	INTERNAL ANT. / UART ON / UART 3.3V	1.0

Date: Friday, October 11, 2019 Sheet 2 of 4

▣ BoT-nLE521 REF. APPLICATION - UART 5V level input

■ Example Schematic

■ INTERNAL ANTENNA
■ UART 5V level input
■ Bypass in Bluetooth connected state
■ Default LDO Mode
■ Default Internal 32.768KHz Mode
■ UART ON
■ WAKE UP

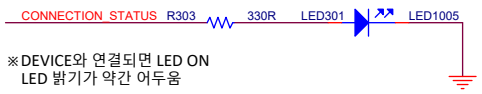


CONNECTION_STATUS LED OPTION

■ CONNECTION STATE

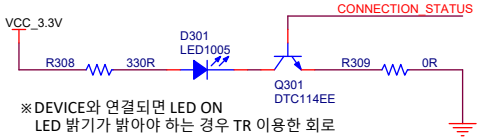
OUTPUT	DESCRIPTION
HIGH	DEVICE CONNECTION
LOW	DEVICE DISCONNECTION

■ EXAMPLE 1



※DEVICE와 연결되면 LED ON
LED 밝기가 약간 어두움

■ EXAMPLE 2



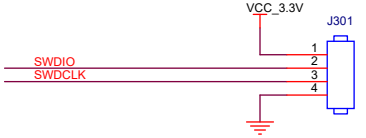
※DEVICE와 연결되면 LED ON
LED 밝기가 밝아야 하는 경우 TR 이용한 회로

FACTOTY_RST

※FACTOTY_RST

DEFAULT SETTING은 INPUT 설정
4초 이상 HIGH 유지시 +OK 응답 후 공장초기화 상태로 복귀시킨다.

J-LINK DEBUG PORT



※ Wireless Certification

무선 인증 진행 시 DTM F/W Download Port

ENTER SLEEP /WAKEUP

※ WAKE UP

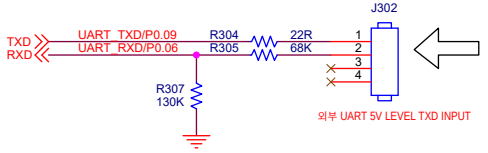
LOW INPUT : 저전력 모드로 들어가지 않고 동작상태

UART ON/OFF

※UART ON

LOW INPUT : UART ON (ENABLE) 상태

UART PORT



※UART Port for SIG / Wireless Certification

무선 인증 진행 시 DTM F/W로 주파수 컨트롤 시 UART를 사용
반드시 라인 절체할 수 있는 저항 필수 추가

AT_COMMAND/ BYPASS

■ BYPASS MODE

LOW INPUT : BYPASS MODE (DATA 전송 모드)

※DEVICE와 연결되기 전에는 AT COMMAND MODE로 동작

※DEVICE와 연결 후 UART MODE PIN HIGH,LOW로 UART MODE 동작 결정

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Title	BoT-nLE521 REF. APPLICATION	
Size A3	Document Number INTERNAL ANT. / UART ON / UART 5V	Rev 1.0
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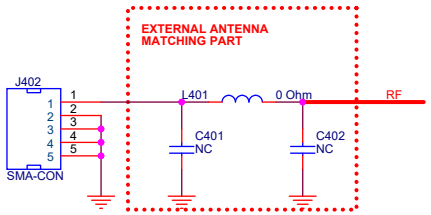
▣ BoT-nLE521 REF. APPLICATION - EXTERNAL ANTENNA / UART 3.3V LEVEL INPUT

■ Example Schematic

■ EXTERNAL ANTENNA
■ UART 3.3V level input
■ Bypass in Bluetooth connected state
■ Default LDO Mode
■ Default Internal 32.768KHz Mode
■ Not Used WAKE

EXTERNAL ANTENNA

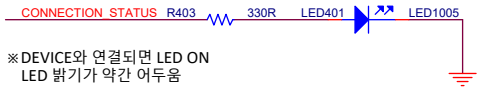


CONNECTION_STATUS LED OPTION

■ CONNECTION STATE

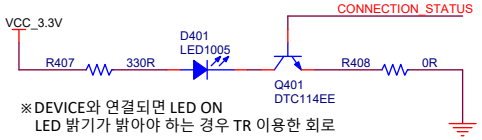
OUTPUT	DESCRIPTION
HIGH	DEVICE CONNECTION
LOW	DEVICE DISCONNECTION

■ EXAMPLE 1



※DEVICE와 연결되면 LED ON
LED 밝기가 약간 어두움

■ EXAMPLE 2

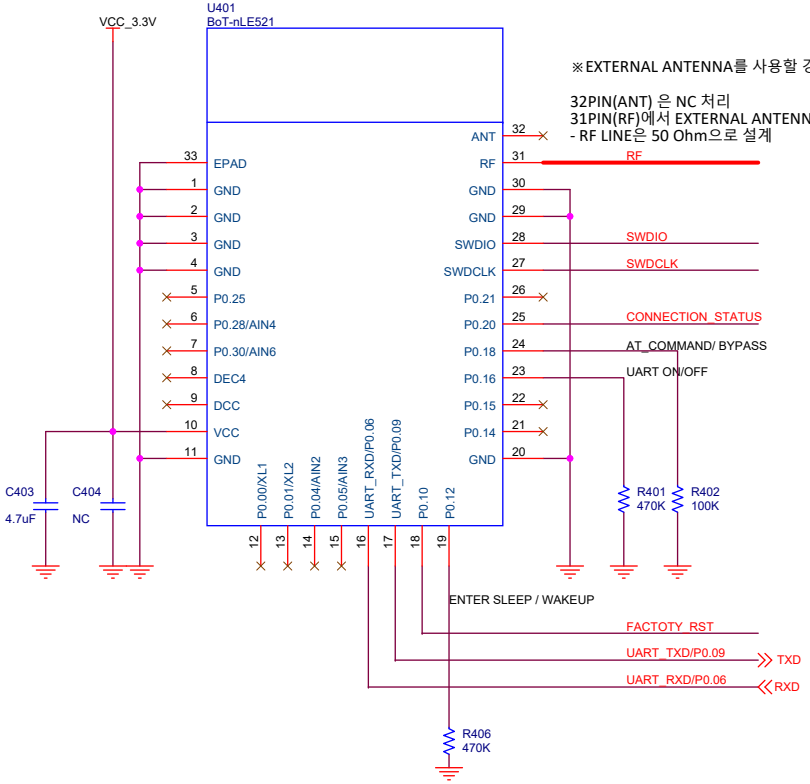


※DEVICE와 연결되면 LED ON
LED 밝기가 밝아야 하는 경우 TR 이용한 회로

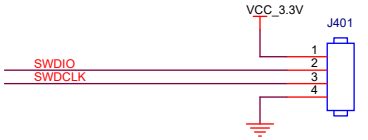
FACTOTY_RST

※FACTOTY_RST

DEFAULT SETTING은 INPUT 설정
4초 이상 HIGH 유지시 +OK 응답 후 공장초기화 상태로 복귀시킨다.



J-LINK DEBUG PORT



※ Wireless Certification

무선 인증 진행 시 DTM F/W Download Port

ENTER SLEEP /WAKEUP

※ WAKE UP

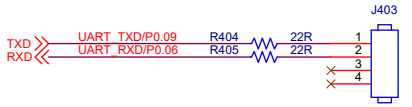
LOW INPUT : 저전력 모드로 들어가지 않고 동작상태

UART ON/OFF

※UART ON

LOW INPUT : UART ON (ENABLE) 상태

UART PORT



※UART Port for SIG / Wireless Certification

무선 인증 진행 시 DTM F/W로 주파수 컨트롤 시 UART를 사용
반드시 라인 절체할 수 있는 저항 필수 추가

AT_COMMAND/ BYPASS

■ BYPASS MODE

LOW INPUT : BYPASS MODE (DATA 전송 모드)

※DEVICE와 연결되기 전에는 AT COMMAND MODE로 동작

※DEVICE와 연결 후 UART MODE PIN HIGH,LOW로 UART MODE 동작 결정

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