MCDP6000C1

Register Specification

KRS-MCDP6000-C1100

Rev. 1.0.0

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Contents

1. TWI Device ID

The Two Wire Interface (TWI) of the MCDP6000 operates as the slave compatible with I2C master. Four device IDs can be supported. Each device's ID is determined by the TWISLV0 and TWISLV1 pins as shown in the table below. The TWISLV0/1 pull-up/down status is detected by the MCDP6000 during the power-up sequence.

Table 1. TWI Device ID Configuration

I2CSLV1	I2CSLV0	Slave ID
Pulled down to Ground	Pulled down to Ground	0x14
Pulled down to Ground	Pulled up to 1.8V	0x15
Pulled up to 1.8V	Pulled down to Ground	0x16
Pulled up to 1.8V	Pulled up to 1.8V	0x17

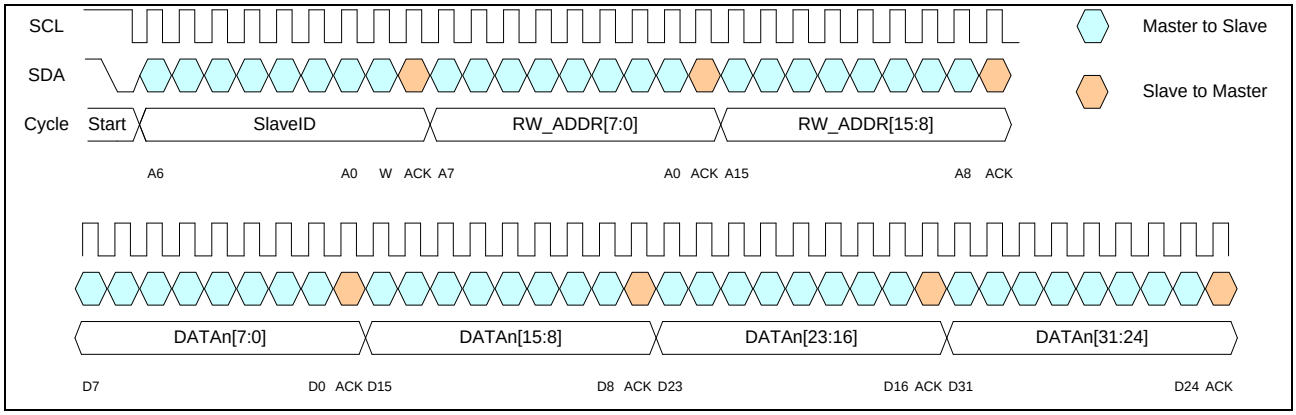
2. TWI Access

The TWI access to the MCDP6000 is 32-bit write or read. All register accesses are on 32-bit word boundaries. Address auto-increment is also allowed on 32-bit word boundary. Stop / Repeated start can be used to change the base address to a new address definition.

The figure below shows typical write access:

1. Master sends device ID with write access.
2. Master sends lower byte of 16-bit register address.
3. Master sends higher bytes of 16-bit register address.
4. Master sends data bytes to be written in order of lower byte to higher byte.

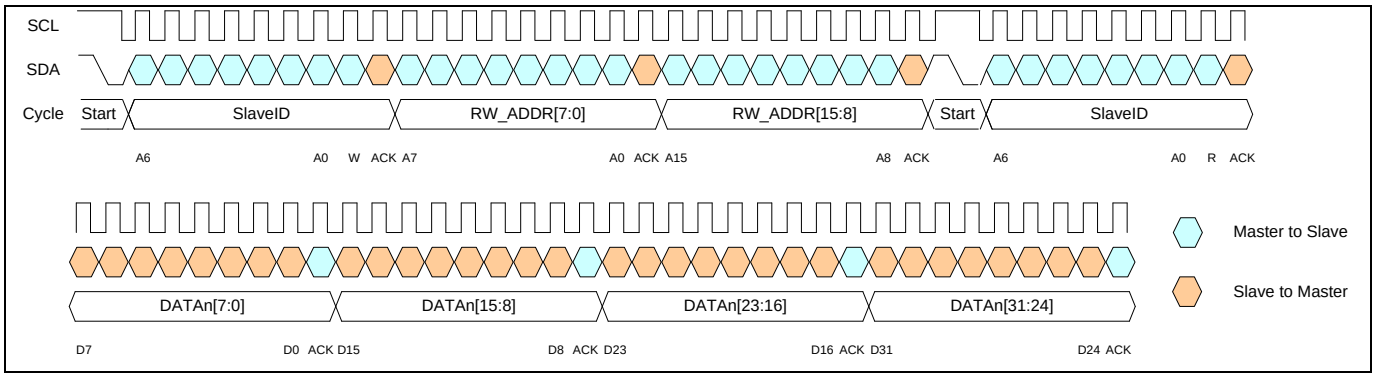
Figure 1. Write Access



The figure below shows typical read access:

1. Master sends device ID with write access.
2. Master sends lower byte of 16-bit register address.
3. Master sends higher bytes of 16-bit register address.
4. Master sends re-start with read access.
5. Slave responds with data bytes.

Figure 2. Read Access



3. TWI Register

3.1. Address Mapping

The registers in “Off” domain needs to be programmed whenever the MCDP6000 exits from “Disabled” state.

Base ADDRESS	REGISTER BANK	Power Domain
0x0000-0x00FF	Reserved	
0x0100	All DPRX	
0x0200	All DPTX	
0x0300	RETIMER_CONFIFG	On (Always-on)
0x0400-0x04FF	Reserved	
0x0500	MFP	On (Always-on)
0x0600-0x06FF	Reserved	
0x0700	DPCD_SNOOP	Off
0x0800-0x08FF	Reserved	
0x0900	LT_CONFIG	Off
0x0A00	DPCD_LTTPR_CAP_ID	Off
0x0B00	DPCD_LTTPR_CONF_STATUS	Off
0x0C00 – 0x0FFF	Reserved	
0x1000	UFP USBRX	On (Always-on)
0x1100	UFP USBTX	On (Always-on)
0x1200	UFP DPRX ML0	Off
0x1300	UFP DPRX ML1	Off
0x1400	UFP DPRX ML2	Off
0x1500	UFP DPRX ML3	Off
0x1600	UFP AUXCH	Off
0x1700-0x1FFF	Reserved	
0x2000	DFP USBRX1	On (Always-on)
0x2100	DFP USBRX2	On (Always-on)
0x2200	DFP DPTX1	Off
0x2300	DFP DPTX2	Off
0x2400	DFP USBDPTX1	On (Always-on)
0x2500	DFP USBDPTX2	On (Always-on)
0x2600	DFP_AUXCH	Off
0x2700-0x27FF	Reserved	
0x2800	MISC_ANALOG	On (Always-on)

Register bank in always on domain retains the values even when MCDP6000 is in “Disabled” state. Register bank in power off domain reset the values upon the wake-up from “Disabled” state.

3.2. Register Specification Listing Definitions

PA	Pending and active read write bit. The pending register is transferred to the active register on an update event. Only the active register contents shall affect chip functionality. The active register bits are cleared to '0', unless otherwise specified, by a software reset or a hardware reset. The pending register bits are only cleared by a hardware reset, and may be overwritten at any time.
RW	Direct read write bit. The register contents affect chip functionality immediately after being written to. A software reset will not clear registers of this type. A hardware reset will clear these registers to '0', unless otherwise specified.
CRW	Self clearing direct read write bit. These are the same as the direct read write bits except they are cleared to '0' by an event specific to each bit.
CRO	Clearable read only bit. These are read only registers that may be cleared to '0' when overwritten with a '1'. This type is most commonly used for interrupt status registers. These are cleared to '0' by both software and a hardware reset.
RO	Read only status bit.
WO	This is a write only register space. A read will yield all zeros.

3.3. Register List

3.3.1. IC Status / Configuration

0x30C	IC_RT_CONFIG	RW
POD: 0x005FFC03		
BIT	**BIT NAME**	**FUNCTION**
15:0	Reserved	Reserved
16	USB_G2_MODE_SEL	USB Gen2 operation mode selection 0: Proprietary operation mode 1: Spec compliant operation mode
19:17	Reserved	Reserved
20	FAST_U2_EXIT_EN	0: 1msec exit time for Phy, but the U2 power is less than 1mW 1: 300usec exit time for Phy, but the U2 power is about a few mW (default)
29:21	Reserved	Reserved
30	XTAL_REF_MODE	0: Normal operation (crystal driven mode) (Default) 1: Single-end reference clock receiver mode
31	REFOUT_EN	REFOUT enable. Active high. 0: Disable REFOUT (Default) 1: Enable REFOUT

0x350	DP_RT_CONFIG	RW
POD: 0x0000000F		
BIT	**BIT NAME**	**FUNCTION**
3:0	DP_RXEQ_CONT	DP Rx EQ adaptation option for [0] RBR, [1] HBR, [2] HBR2, [3] HBR3 0: Rx EQ adaptation during TPS2-4 (Default) 1: Rx EQ adaptation during TPS2-4 and the beginning of Video stream
4	RTMR_DP_AUX_CONFIG	0: Low latency mode (Default) 1: Normal latency mode
6:5	Reserved	Reserved
7	DPRX_RST_CONFIG	0: initialize DPRX upon DPCD 100h and 600h write acknowledgement (Default) 1: disable DPRX initialization based on DPCD 100h and 600h
8	Reserved	Reserved
9	RETIMER_CONFIG_RW9	Bootstrap override enable for RTMR_DP_AUX_CONFIG[0]
31:10	Reserved	Reserved

0x0504	OPMODE_CONF	RW
POD: 0x0000002E		

BIT	BIT NAME	FUNCTION
0	Reserved	
1	PPOL_OVR_EN	P_POL_OVR_EN, 0: GPIO setting, 1: I2C setting
2	PCONF0_OVR_EN	P_CONF0_OVR_EN, 0: GPIO setting, 1: I2C setting
3	PCONF1_OVR_EN	P_CONF1_OVR_EN, 0: GPIO setting, 1: I2C setting
4	PPOL	P_POL
5	PCONF0	P_CONF0
6	PCONF1	P_CONF1
7	Reserved	
8	IC_SOFT_RST	0: Normal operation 1: Reset IC except for registers
9	USB_SOFT_RST	0: Normal operation 1: Reset USB data path
10	DP_SOFT_RST	0: Normal operation 1: Reset DP data path
11	DP_AUX_SOFT_RST	0: Normal operation 1: Reset DP data path
12	PPOL_BS_OVR	Bootstrap override enable for P_POL
13	PCONF0_BS_OVR	Bootstrap override enable for P_CONF0
14	PCONF1_BS_OVR	Bootstrap override enable for P_CONF1
15	Reserved	
16	DP_LT_AMP_PRE_CHK_DIS	0: Enable EQ adaptation result check to request different voltage swing or pre-emphasis level 1: Disable EQ adaptation result check during DP link training
17	DP_LT_SYMB_ERR_CHK_DIS	0: Enable symbol error count check to request different voltage swing or pre-emphasis level 1: Disable symbol error count check during DP link training
31:18	Reserved	Reserved

0x510	IC_REV	RO
IC Revision		

BIT	BIT NAME	FUNCTION
0	TWISLV0_BS_STATUS	Bootstrap status of TWISLV0 pin
1	TWISLV1_BS_STATUS	Bootstrap status of TWISLV1 pin
2	P_CONF0_BS_STATUS	Bootstrap status of P_CONF0 pin
3	P_CONF1_BS_STATUS	Bootstrap status of P_CONF1 pin
4	P_POL_BS_STATUS	Bootstrap status of P_POL pin
5	TM_BS_STATUS	Bootstrap status of TM pin
7:6	Reserved	
11:8	MINOR_VERSION	2h for C1
15:12	MAJOR_VERSION	3h for C1
31:16	Reserved	Reserved

0x281C	RO_TUNE_MANUAL	RW
POD: 0x18080000		

BIT	BIT NAME	FUNCTION
25:0	Reserved	Reserved
26	RO_CTUNE_SEL	Coarse and fine tune ranges selection. 0h : Normal mode (Ring Oscillator frequency is determined by bit[5:2] of 0x283C) 1h : Manual mode (Ring Oscillator frequency is determined by bit[30:27] of 0x281C)
30:27	RO_RC_TRIM	RO frequency adjustment
31	Reserved	Reserved

0x283C	RO_CTUNE_STATUS	RO
POD: 0x00000000		

BIT	BIT NAME	FUNCTION
0	RO_CTUNE_DONE	Status indicating whether tune is done. High active. It is cleared when tune is restarted.
1	RO_LD_LOCK	Status indicating whether PLL is locked. 0h : Loss of lock 1h : Lock It is valid when VCO settling time is over after clamp is released since CTUNE_DONE becomes high.
3:2	RO_CTUNEF_MON	Fine tune status
5:4	RO_CTUNEC_MON	Coarse tune status
31:6	Reserved	Reserved

3.3.2. USB Status Monitor

0x320	USB_RTSSM_STATUS0	RO
POD: 0x00000000		
BIT	**BIT NAME**	**FUNCTION**
22:0	USB_RTSSM0_CPU	RTSSM status (one hot) Bit 0 – Rx.Detect Bit 1 – Polling.SpeedDetect Bit 2 – Polling.PortConfig Bit 3 – Polling.RxEQ Bit 4 – Polling.TSx Bit 5 – Polling.Idle Bit 6 – Compliance Mode Bit 7 – U0 Bit 8 – U1 Bit 9 – Recovery.TSx Bit 10 – Recovery.Idle Bit 11 – PassThrough Loopback Bit 12 – Local Loopback.Active Bit 13 – Local Loopback.Exit Bit 14 – Hot Reset Bit 15 – BLR Compliance Mode Bit 16 – Rx.Detect Bit 17 – DCI Bit 18 – U1 Bit 19 – U2 Bit 20 – U3 Bit 21 – Idle Bit 22 – Idle LP
23	USB_P0_RATE	0: Gen1 (SS), 1: Gen2 (SSP)
31:24	Reserved	Reserved

0x324	USB_RTSSM_STATUS1	RO
POD: 0x00000000		
BIT	**BIT NAME**	**FUNCTION**
22:0	USB_RTSSM1_TYPEC	RTSSM status (one hot) Bit 0 – Rx.Detect Bit 1 – Polling.SpeedDetect Bit 2 – Polling.PortConfig Bit 3 – Polling.RxEQ Bit 4 – Polling.TSx Bit 5 – Polling.Idle Bit 6 – Compliance Mode Bit 7 – U0 Bit 8 – U1 Bit 9 – Recovery.TSx Bit 10 – Recovery.Idle Bit 11 – PassThrough Loopback Bit 12 – Local Loopback.Active Bit 13 – Local Loopback.Exit

		Bit 14 – Hot Reset Bit 15 – BLR Compliance Mode Bit 16 – Rx.Detect Bit 17 – DCI Bit 18 – U1 Bit 19 – U2 Bit 20 – U3 Bit 21 – Idle Bit 22 – Idle LP
23	USB_P1_RATE	0: Gen1 (SS), 1: Gen2 (SSP)
31:24	Reserved	Reserved

0x328	USB_RTSSM_STATUS2	CRO
POD: 0x00000000		
BIT	**BIT NAME**	**FUNCTION**
3:0	USB_P0_RXDET_HIS	The number of USB Rx Detect state transition
7:4	USB_P0_POLSPD_HIS	The number of USB Polling.SpeedDetect state transition
11:8	USB_P0_POLPORT_HIS	The number of USB Polling.PortConfig state transition
15:12	USB_P0_POLRXEQ_HIS	The number of USB Polling.RxEQ state transition
19:16	USB_P0_POLTSX_HIS	The number of USB Polling.TSx state transition
23:20	USB_P0_POLIDLE_HIS	The number of USB Polling.Idle state transition
27:24	USB_P0_COMPL_HIS	The number of USB Compliance Mode state transition
31:28	USB_P0_U0_HIS	The number of USB U0 state transition

0x32C	USB_RTSSM_STATUS3	CRO
POD: 0x00000000		
BIT	**BIT NAME**	**FUNCTION**
3:0	USB_P0_U1_HIS	The number of USB U1 state transition
7:4	USB_P0_U2_HIS	The number of USB U2 state transition
11:8	USB_P0_U3_HIS	The number of USB U3 state transition
15:12	USB_P0_RECTSX_HIS	The number of USB Recovery.TSx state transition
19:16	USB_P0_RECIDLE_HIS	The number of USB Recovery Idle state transition
23:20	USB_P0_PTLB_HIS	The number of USB PassThrough Loopback state transition
27:24	USB_P0_LLACT_HIS	The number of USB Local Loopback.Active state transition
31:28	USB_P0_LLEXIT_HIS	The number of USB Local Loopback.Exit state transition

0x330	USB_RTSSM_STATUS4	CRO
POD: 0x00000000		
BIT	**BIT NAME**	**FUNCTION**
3:0	USB_P1_RXDET_HIS	The number of USB Rx Detect state transition
7:4	USB_P1_POLSPD_HIS	The number of USB Polling.SpeedDetect state transition

11:8	USB_P1_POLPORT_HIS	The number of USB Polling.PortConfig state transition
15:12	USB_P1_POLRXEQ_HIS	The number of USB Polling.RxEQ state transition
19:16	USB_P1_POLTSX_HIS	The number of USB Polling.TSx state transition
23:20	USB_P1_POLIDLE_HIS	The number of USB Polling.Idle state transition
27:24	USB_P1_COMPL_HIS	The number of USB Compliance Mode state transition
31:28	USB_P1_U0_HIS	The number of USB U0 state transition

0x334	USB_RTSSM_STATUS5	CRO
POD: 0x00000000		
BIT	**BIT NAME**	**FUNCTION**
3:0	USB_P1_U1_HIS	The number of USB U1 state transition
7:4	USB_P1_U2_HIS	The number of USB U2 state transition
11:8	USB_P1_U3_HIS	The number of USB U3 state transition
15:12	USB_P1_RECTSX_HIS	The number of USB Recovery.TSx state transition
19:16	USB_P1_RECIDLE_HIS	The number of USB Recovery Idle state transition
23:20	USB_P1_PTLB_HIS	The number of USB PassThrough Loopback state transition
27:24	USB_P1_LLACT_HIS	The number of USB Local Loopback.Active state transition
31:28	USB_P1_LLEXIT_HIS	The number of USB Local Loopback.Exit state transition

0x338	USB_RTSSM_STATUS6	CRO
POD: 0x00000000		
BIT	**BIT NAME**	**FUNCTION**
3:0	USB_P0_HRST_HIS	The number of USB Hot Reset state transition
7:4	USB_P0_BLRC_HIS	The number of USB BLR Compliance state transition
15:8	Reserved	Reserved
19:16	USB_P1_HRST_HIS	The number of USB Hot Reset state transition
23:20	USB_P1_BLRC_HIS	The number of USB BLR Compliance state transition
31:24	Reserved	Reserved

3.3.3. DisplayPort Receiver Logic Register

0x61C	DPRX_ERR_CNT_CTRL	RW
POD: 0x00000001		
Symbol Error Counter Clear bit		
BIT	**BIT NAME**	**FUNCTION**
0	DPRX_ERR_CNT_EN	1 – enable symbol error counters; 0 – clear counters
31:1	Reserved	Reserved

0x62C	DP_LT_STATUS	RO
POD: 0x00000000		

BIT	BIT NAME	FUNCTION
5:0	DPRX_FINAL_LINK_BW	DPRX Link BW after Link Training
7:6	Reserved	Reserved
10:8	DPRX_FINAL_LANE_COUNT	1 = one lane; 2 – two lanes; 4 – four lanes
12:11	Reserved	Reserved
13	DPRX_FINAL_ENH_EN	Final setting 0 = Enhanced Framing symbol sequence not enabled; 1 = Enhanced symbol sequence for BS, SR, CPBS and CPSR
16:14	DPRX_CURR_LT_PATRN	000 – Training not in progress; 001 – Training pattern 1 (D10.2); 010 – Training pattern 2; 011 – Training pattern 3; 1xx – Reserved
31:17	Reserved	Reserved

0x660	DPRX_CONTROL	RW
POD: 0x00001001		

BIT	BIT NAME	FUNCTION
0	DPRX_EN	Common DPRX enable signal. When it is 0 then all blocks are disabled.
3:1	Reserved	
4	ALIGN_CTLR	0: Interlane alignment is done in DPRX logic 1: Interlane alignment is done in DPRX PHY
11:5	Reserved	Reserved
12	DPRX_FEFIFO_RESET_AUTO_EN	FEFIFO will be reset automatically when alignment error(s) are detected
13	Reserved	Reserved
14	LTTPR_FIFO_GATING	LTTPR ML output during LTTPR LT. 0: gated, 1: forwarded
31:15	Reserved	Reserved

0x67C	DP_FIFO_CTRL	RW
POD: 0x00000003		

BIT	BIT NAME	FUNCTION
0	ALIGNED_DATA_SEL	0 = Recovered Link Symbol Data from ANALOG PHY 1 = Aligned Locked Symbol Data from DP Digital PHY
1	DPTX_SKEW_CTLR	0 = Data is forwarded as DPRX PHY receives 1 = Data is skewed based on the alignment logic output (bit 4 of 0x660.) Set 1 when 0x660[4] is set to 0
31:2	Reserved	Reserved

3.3.4. DPCD_SNOOP

0x0700	DPCD_SNOOP_0	RW
(Snoop DPCD 102 – 105) (DPCD ADDR F0240, F01F0, F01A0, F0150, F0100, F00B0, F0060, F0010h same as DPCD00102h) bits 7:0 (DPCD ADDR F0241, F01F1, F01A1, F0151, F0101, F00B1, F0061, F0011h same as DPCD00103h) bits 15:8 (DPCD ADDR F0242, F01F2, F01A2, F0152, F0102, F00B2, F0062, F0012h same as DPCD00104h) bits 23:16 (DPCD ADDR F0243, F01F3, F01A3, F0153, F0103, F00B3, F0063, F0013h same as DPCD00105h) bits 31:24		

BIT	BIT NAME	FUNCTION
3:0	training_pattern_selection	TRAINING_PATTERN_SET_PHY_REPEATER1 Link Training Pattern Selection. 0000 = Training not in progress (or disabled). 0001 = Link Training Pattern Sequence 1. 0010 = Link Training Pattern Sequence 2. 0011 = Link Training Pattern Sequence 3. 0111 = Link Training Pattern Sequence 4. All other values are RESERVED.
4	recovered_clock_out_en	0 = Recovered clock output from a test pad of DP RX is not enabled. 1 = Recovered clock output from a test pad of DP RX enabled.
5	scrambling_disable	0 = DPTX scrambles data symbols before transmission. 1 = DPTX disables scrambler and transmits all symbols without scrambling.
7:6	symbol_error_count_sel	00 = Count Disparity and Illegal Symbol errors 01 = Count Disparity errors only 10 = Count Illegal Symbol errors only 11 = RESERVED
9:8	voltage_swing_set_lane0	TRAINING_LANE0_SET -VOLTAGE SWING SET 00 = Voltage swing level 0. 01 = Voltage swing level 1. 10 = Voltage swing level 2. 11 = Voltage swing level 3.
10	max_swing_reached_lane0	MAX_SWING_REACHED The transmitter must support at least three levels of voltage swing (levels 0, 1 and 2). If only three levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 10 (level 2)), then this bit must be set to 1, and cleared in all other cases. If all four levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 11 (level 3)), then this bit must be set to 1,and cleared in all other cases.
12:11	pre_emphasis_set_lane0	PRE-EMPHASIS_SET 00 = Pre-emphasis level 0. 01 = Pre-emphasis level 1.

		10 = Pre-emphasis level 2. 11 = Pre-emphasis level 3.
13	max_pre_emphasis_reached_lane0	MAX_PRE-EMPHASIS_REACHED The transmitter must support at least three levels of pre-emphasis (levels 0, 1 and 2). Support of additional pre-emphasis level is optional. If only three levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10 (level 2)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. If all four levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11 (level 3)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. Support of independent pre-emphasis level control for each lane is also optional.
15:14	Reserved	RESERVED
17:16	voltage_swing_set_lane1	TRAINING_LANE1_SET -VOLTAGE SWING SET 00 = Voltage swing level 0. 01 = Voltage swing level 1. 10 = Voltage swing level 2. 11 = Voltage swing level 3.
18	max_swing_reached_lane1	MAX_SWING_REACHED The transmitter must support at least three levels of voltage swing (levels 0, 1 and 2). If only three levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 10 (level 2)), then this bit must be set to 1, and cleared in all other cases. If all four levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 11 (level 3)), then this bit must be set to 1,and cleared in all other cases.
20:19	pre_emphasis_set_lane1	PRE-EMPHASIS_SET 00 = Pre-emphasis level 0. 01 = Pre-emphasis level 1. 10 = Pre-emphasis level 2. 11 = Pre-emphasis level 3.
21	max_pre_emphasis_reached_lane1	MAX_PRE-EMPHASIS_REACHED The transmitter must support at least three levels of pre-emphasis (levels 0, 1 and

		2). Support of additional pre-emphasis level is optional. If only three levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10 (level 2)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. If all four levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11 (level 3)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. Support of independent pre-emphasis level control for each lane is also optional.
23:22	Reserved	RESERVED
25:24	voltage_swing_set_lane2	TRAINING_LANE1_SET -VOLTAGE SWING SET 00 = Voltage swing level 0. 01 = Voltage swing level 1. 10 = Voltage swing level 2. 11 = Voltage swing level 3.
26	max_swing_reached_lane2	MAX_SWING_REACHED The transmitter must support at least three levels of voltage swing (levels 0, 1 and 2). If only three levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 10 (level 2)), then this bit must be set to 1, and cleared in all other cases. If all four levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 11 (level 3)), then this bit must be set to 1,and cleared in all other cases.
28:27	pre_emphasis_set_lane2	PRE-EMPHASIS_SET 00 = Pre-emphasis level 0. 01 = Pre-emphasis level 1. 10 = Pre-emphasis level 2. 11 = Pre-emphasis level 3.
29	max_pre_emphasis_reached_lane2	MAX_PRE-EMPHASIS_REACHED The transmitter must support at least three levels of pre-emphasis (levels 0, 1 and 2). Support of additional pre-emphasis level is optional. If only three levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10 (level 2)), then the transmitter must set

		this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. If all four levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11 (level 3)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. Support of independent pre-emphasis level control for each lane is also optional.
31:30	Reserved	RESERVED

0x0704	DPCD _SNOOP_1	RW
(Snoop 106) (DPCD ADDR F0244, F01F4, F01A4, F0154, F0103, F00B4, F0064, F0014h same as DPCD00106h) TRAINING_LANE3_SET bits 7:0 (DPCD ADDR F0015h same as DPCD0010Bh) LINK_QUAL_LANE0_SET bits 15:8 (DPCD ADDR F0016h same as DPCD0010Ch) LINK_QUAL_LANE1_SET bits 23:8 (DPCD ADDR F0017h same as DPCD0010Dh) LINK_QUAL_LANE2_SET bits 31:24		
BIT	**BIT NAME**	**FUNCTION**
1:0	voltage_swing_set_lane3	TRAINING_LANE0_SET -VOLTAGE SWING SET 00 = Voltage swing level 0. 01 = Voltage swing level 1. 10 = Voltage swing level 2. 11 = Voltage swing level 3.
2	max_swing_reached_lane3	MAX_SWING_REACHED The transmitter must support at least three levels of voltage swing (levels 0, 1 and 2). If only three levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 10 (level 2)), then this bit must be set to 1, and cleared in all other cases. If all four levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 11 (level 3)), then this bit must be set to 1,and cleared in all other cases.
4:3	pre_emphasis_set_lane3	PRE-EMPHASIS_SET 00 = Pre-emphasis level 0. 01 = Pre-emphasis level 1. 10 = Pre-emphasis level 2. 11 = Pre-emphasis level 3.
5	max_pre_emphasis_reached_lane3	MAX_PRE-EMPHASIS_REACHED The transmitter must support at least three levels of pre-emphasis (levels 0, 1 and

		2). Support of additional pre-emphasis level is optional. If only three levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10 (level 2)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. If all four levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11 (level 3)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. Support of independent pre-emphasis level control for each lane is also optional.
7:6	Reserved	RESERVED
10:8	link_qual_pattern_set_lane0	LINK_QUAL_LANE0_SET Must be cleared to 00h upon power-on reset or an upstream device disconnect. The controls in this register supersede the controls in the TRAINING_PATTERN_SET register (DPCD Address 00102h). LINK_QUAL_PATTERN_SET 000 = Link quality test pattern not transmitted. 001 = D10.2 test pattern (unscrambled) transmitted (same as Link Training Pattern Sequence 1). 010 = Symbol Error Rate Measurement Pattern transmitted. 011 = PRBS7 transmitted. 100 = 80-bit custom pattern transmitted. 101 = CP2520 (HBR2 Compliance EYE pattern) transmitted. 110, 111 = RESERVED.
15:11	Reserved	RESERVED
18:16	link_qual_pattern_set_lane1	LINK_QUAL_LANE1_SET Must be cleared to 00h upon power-on reset or an upstream device disconnect. The controls in this register supersede the controls in the TRAINING_PATTERN_SET register (DPCD Address 00102h). LINK_QUAL_PATTERN_SET 000 = Link quality test pattern not transmitted. 001 = D10.2 test pattern (unscrambled) transmitted (same as Link Training Pattern Sequence 1). 010 = Symbol Error Rate Measurement Pattern transmitted. 011 = PRBS7 transmitted. 100 = 80-bit custom pattern transmitted.

		101 = CP2520 (HBR2 Compliance EYE pattern) transmitted. 110, 111 = RESERVED.
23:19	Reserved	RESERVED
26:24	link_qual_pattern_set_lane2	LINK_QUAL_LANE2_SET Must be cleared to 00h upon power-on reset or an upstream device disconnect. The controls in this register supersede the controls in the TRAINING_PATTERN_SET register (DPCD Address 00102h). LINK_QUAL_PATTERN_SET 000 = Link quality test pattern not transmitted. 001 = D10.2 test pattern (unscrambled) transmitted (same as Link Training Pattern Sequence 1). 010 = Symbol Error Rate Measurement Pattern transmitted. 011 = PRBS7 transmitted. 100 = 80-bit custom pattern transmitted. 101 = CP2520 (HBR2 Compliance EYE pattern) transmitted. 110, 111 = RESERVED.
31:27	Reserved	RESERVED

0x0708	**DPCD_SNOOP_2**	**RW**
(DPCD ADDR F0018h same as DPCD0010Eh) LINK_QUAL_LANE3_SET bits 7:0		
BIT	**BIT NAME**	**FUNCTION**
2:0	link_qual_pattern_set_lane3	LINK_QUAL_LANE3_SET Must be cleared to 00h upon power-on reset or an upstream device disconnect. The controls in this register supersede the controls in the TRAINING_PATTERN_SET register (DPCD Address 00102h). LINK_QUAL_PATTERN_SET 000 = Link quality test pattern not transmitted. 001 = D10.2 test pattern (unscrambled) transmitted (same as Link Training Pattern Sequence 1). 010 = Symbol Error Rate Measurement Pattern transmitted. 011 = PRBS7 transmitted. 100 = 80-bit custom pattern transmitted. 101 = CP2520 (HBR2 Compliance EYE pattern) transmitted. 110, 111 = RESERVED.
31:3	Reserved	RESERVED

0x0720	DPCD_SNOOP_3	RW

LT_DPCD_SNOOP
(DPCD ADDR F0030h same as DPCD00202h and DPCD0200Ch) LANE0_1_STATUS bits 7:0
(DPCD ADDR F0031h same as DPCD00203h and DPCD0200Dh) LANE2_3_STATUS bits 15:8
(DPCD ADDR F0032h same as DPCD00204h and DPCD0200Eh) LANE_ALIGN_STATUS bits 23;16
(DPCD ADDR F0033h same as DPCD00206h) ADJUST_REQ_LANE0_1_STATUS bits 31:24

BIT	BIT NAME	FUNCTION
0	Lane0_cr_done	LANE0_CR_DONE (for AUX Read Only)
1	Lane0_eq_done	LANE0_EQ_DONE (for AUX Read Only)
2	Lane0_sym_locked	LANE0_SYM_LOCKED (for AUX Read Only)
3	Reserved	Reserved
4	Lane1_cr_done	LANE1_CR_DONE (for AUX Read Only)
5	Lane1_eq_done	LANE1_EQ_DONE (for AUX Read Only)
6	Lane1_sym_locked	LANE1_SYM_LOCKED (for AUX Read Only)
7	Reserved	Reserved
8	Lane2_cr_done	LANE2_CR_DONE (for AUX Read Only)
9	Lane2_eq_done	LANE2_EQ_DONE (for AUX Read Only)
10	Lane2_sym_locked	LANE2_SYM_LOCKED (for AUX Read Only)
11	Reserved	Reserved
12	Lane3_cr_done	LANE3_CR_DONE (for AUX Read Only)
13	Lane3_eq_done	LANE3_EQ_DONE (for AUX Read Only)
14	Lane3_sym_locked	LANE3_SYM_LOCKED (for AUX Read Only)
15	Reserved	Reserved
23:16	Lane_align_status_updated	LANE_ALIGN_STATUS_UPDATED
25:24	Volt_swing_lane0	**VOLT_SWING_LANE0** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
27:26	Pre_emp_lane0	**PRE_EMP_LANE0** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
29:28	Volt_swing_lane1	**VOLT_SWING_LANE1** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
31:30	Pre_emp_lane1	**PRE_EMP_LANE1** 00 = Level 0 01 = Level 1 10 = Level 2

		11 = Level 3

0x0724	DPCD_SNOOP_4	RW
(DPCD ADDR F0034h same as DPCD00207h) ADJUST_REQ_LANE2_3_STATUS bits 7:0 (DPCD ADDR F0035h same as DPCD00210h) SYMBOL_ERROR_COUNT_LANE_L0 bits 15:8 (DPCD ADDR F0036h same as DPCD00211h) SYMBOL_ERROR_COUNT_LANE_H0 bits 23:16 (DPCD ADDR F0037h same as DPCD00212h) SYMBOL_ERROR_COUNT_LANE_L1 bits 31:24		
BIT	**BIT NAME**	**FUNCTION**
1:0	Volt_swing_lane2	VOLT_SWING_LANE2 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
3:2	Pre_emp_lane2	PRE_EMP_LANE2 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
5:4	Volt_swing_lane3	VOLT_SWING_LANE3 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
7:6	Pre_emp_lane3	PRE_EMP_LANE3 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
15:8	Sym_error_cnt_lane0_l	SYM_ERROR_CNT_LANE0_L
22:16	Sym_error_cnt_lane0_h	SYM_ERROR_CNT_LANE0_H
23	Sym_error_cnt_lan0_v	SYM_ERROR_CNT_LANE0_VALID
31:24	Sym_error_cnt_lane1_l	SYM_ERROR_CNT_LANE1_L

0x0728	DPCD_SNOOP_5	RW
(DPCD ADDR F0038h same as DPCD00213h) SYMBOL_ERROR_COUNT_LANE_H1 bits 7:0 (DPCD ADDR F0039h same as DPCD00214h) SYMBOL_ERROR_COUNT_LANE_L2 bits 15:8 (DPCD ADDR F003Ah same as DPCD00215h) SYMBOL_ERROR_COUNT_LANE_H2 bits 23:16 (DPCD ADDR F003Bh same as DPCD00216h) SYMBOL_ERROR_COUNT_LANE_L3 bits 31:24		
BIT	**BIT NAME**	**FUNCTION**
6:0	Sym_error_cnt_lane1_h	SYM_ERROR_CNT_LANE1_H
7	Sym_error_cnt_lan1_v	SYM_ERROR_CNT_LANE1_V
15:8	Sym_error_cnt_lane2_l	SYM_ERROR_CNT_LANE2_L
22:16	Sym_error_cnt_lane2_h	SYM_ERROR_CNT_LANE2_H
23	Sym_error_cnt_lan2_v	SYM_ERROR_CNT_LANE2_V

31:24	Sym_error_cnt_lane3_l	SYM_ERROR_CNT_LANE3_L

0x072C	DPCD_SNOOP_6	RW
(DPCD ADDR F003Ch same as DPCD00217) SYMBOL_ERROR_COUNT_LANE_H3 bits 7:0 (DPCD ADDR F003Dh) IEEE_OUI_1 bits 15:8 (DPCD ADDR F003Eh) IEEE_OUI_2 bits 23:16 (DPCD ADDR F003Fh) IEEE_OUI_3 bits 31:24		
BIT	**BIT NAME**	**FUNCTION**
6:0	Sym_error_cnt_lane3_h	SYM_ERROR_CNT_LANE3_H
7	Sym_error_cnt_lan3_v	SYM_ERROR_CNT_LANE1_V
15:8	IEEE_OUT1	IEEE_OUT1
23:16	IEEE_OUT2	IEEE_OUT2
31:24	IEEE_OUT3	IEEE_OUT3

0x0750	DPCD_SNOOP_7	RW
(snoop 00002-00000h)		
BIT	**BIT NAME**	**FUNCTION**
7:0	DPRX_DPCD_REV_00000	7:4 Major Rev 3:0 Minor Rev
15:8	MAX_LINK_RATE_00001	Only four values are supported. All other values are RESERVED except for eDP v1.4 (DPCD Rev. 1.3 or lower) and MyDP DPRX. 06h = 1.62Gbps/lane. 0Ah = 2.7Gbps/lane. 14h = 5.4Gbps/lane. 1Eh = 8.1Gbps/lane. eDP v1.4 DPRX (DPCD Rev. 1.3 or lower) can program the MAX_LINK_RATE register value to 00h to indicate that the DPRX supports the Main-Link rates by way of the Link Rate Table method. See eDP v1.4. A MyDP DPRX of an active MyDP converter (either MyDP-to-legacy converter or MyDP-to-DP lane-count converter) can support a value of 19h (6.75Gbps/lane
23:16	MAX_LANE_COUNT_00002	Snoop DPRX Max Lane Count Capability 1h = 1 lane (Lane 0 only) 2h = 2 lanes (Lanes 0 and 1 only) 4h = 4 lanes A Source device may choose any lane count as long as it does not exceed the capability of

31:24	Reserved	Reserved

0x0754	DPCD_SNOOP_8	RW
(snoop 00100h-00101h, 00600h)		
BIT	**BIT NAME**	**FUNCTION**
7:0	LINK_BW_SET_100	Snoop Main Link BW Setting = Value x 0.27Gbps 06h = 1.62 Gbps/lane 0Ah = 2.7 Gbps/lane 14h = 5.4 Gbps/lane 1Eh = 8.1 Gbps/lane
15:8	LANE_COUNT_SET_101	1h = 1 lane (Lane 0 only) snooped 2h = 2 lanes (Lane 0 and 1 only) 4h = 4 lanes
23:16	SET_POWER_STATE_600	**SET_POWER_STATE** Must be programmed to 001 (binary) upon power-on reset or an upstream device disconnect. 001 = Set local Sink device and all downstream Sink devices to D0 (normal operation mode). 010 = Set local Sink device and all downstream Sink devices to D3
31:24	Reserved	Reserved

3.3.5. LT_CONFIG

0x0900	LT_CONFIG_0	RW
POD: 0x00010506		
BIT	**BIT NAME**	**FUNCTION**
3:0	DPRX_AUX_CLK_LOW	Determine Low Period for AUX_CLK=2MHz
7:4	Reserved	Reserved
11:8	DPRX_AUX_CLK_HIGH	Determine High Period for AUX_CLK=2MHz
15:12	Reserved	Reserved
16	DPRX_AUX_CLK_EN	‘1’ AUX_CLK Enable, ‘0’ Disable AUX_CLK
17	Reserved	Reserved
18	AUX_POLARITY	‘0’ set for positive AUX Polarity
24:19	Reserved	Reserved
26:25	AUX_MOD_CTRL	00b: default
27	Reserved	Reserved
31:28	ADJ_REQ_RPT_NUM	Number of adjust request update cycle. 0 : ADJUST_REQUEST set is updated every request 1 : ADJUST_REQUEST set is updated every tow requests

		2 : ADJUST_REQUEST set is updated every three requests …

0x0904	LT_CONFIG_1	RW
POD: 0x66555501		

BIT	BIT NAME	FUNCTION
7:0	LTTPR_RD_INT	Defines 0xF0020[6:0] for TRAINING_AUX_RD_INTERVAL_PHY_REPEATERx
9:8	FORCE_ML0_VSL	ML0 voltage swing level when LT_CONFIG_2.FORCE_TX_PARAM = 1b
11:10	FORCE_ML0_PEL	ML0 pre-emphasis level LT_CONFIG_2.FORCE_TX_PARAM = 1b
13:12	FORCE_ML1_VSL	ML1 voltage swing level when LT_CONFIG_2.FORCE_TX_PARAM = 1b
15:14	FORCE_ML1_PEL	ML1 pre-emphasis level LT_CONFIG_2.FORCE_TX_PARAM = 1b
17:16	FORCE_ML2_VSL	ML2 voltage swing level when LT_CONFIG_2.FORCE_TX_PARAM = 1b
19:18	FORCE_ML2_PEL	ML2 pre-emphasis level LT_CONFIG_2.FORCE_TX_PARAM = 1b
21:20	FORCE_ML3_VSL	ML3 voltage swing level when LT_CONFIG_2.FORCE_TX_PARAM = 1b
23:22	FORCE_ML3_PEL	ML3 pre-emphasis level LT_CONFIG_2.FORCE_TX_PARAM = 1b
31:24	Reserved	Reserved

0x0908	LT_CONFIG_2	RW
POD: 0x00000066		

BIT	BIT NAME	FUNCTION
9:0	Reserved	Reserved
10	FORCE_TX_PARAM	0: Transmitter setting as directed by the link training process 1: Transmitter setting is forced with bit[23:8] of 0x0904 register
11	FULL_TRANSPARENT_EN	0: Pseudo transparent for DPCD206h and DPCD207h in the transparent 1: DPCD 206h 207h pass-through mode
13:12	Reserved	Reserved
14	PRE_EMP_LEVEL_3_DIS	0: PRE_EMP_LEVEL_3 is supported 1: PRE_EMP_LEVEL_3 is not supported
31:16	Reserved	Reserved

0x090C	LT_CONFIG_3	RW
POD: 0x04000000		
BIT	**BIT NAME**	**FUNCTION**
23:0	Reserved	Reserved
30:24	DPRX_RD_INT	Defines 0x0000E[6:0] for Training_AUX-RD_INTERVAL Default value is 4
31	AMP_LEVEL_3_DIS	0: VOLT_SWING_LEVEL_3 is supported 1: VOLT_SWING_LEVEL_3 is not supported

0x0910	LT_CONFIG_4	RW
POD: 0x5A5A5555		
BIT	**BIT NAME**	**FUNCTION**
1:0	ADJ_SWING_REQ_LN0_0	2nd adjust request value of voltage swing level of ML0
3:2	ADJ_SWING_REQ_LN1_0	2nd adjust request value of voltage swing level of ML1
5:4	ADJ_PRE_EMP_REQ_LN0_0	2nd adjust request value of pre-emphasis level of ML0
7:6	ADJ_PRE_EMP_REQ_LN1_0	2nd adjust request value of pre-emphasis level of ML1
9:8	ADJ_SWING_REQ_LN2_0	2nd adjust request value of voltage swing level of ML2
11:10	ADJ_SWING_REQ_LN3_0	2nd adjust request value of voltage swing level of ML3
13:12	ADJ_PRE_EMP_REQ_LN2_0	2nd adjust request value of pre-emphasis level of ML2
15:14	ADJ_PRE_EMP_REQ_LN3_0	2nd adjust request value of pre-emphasis level of ML3
31:16	ADJ_REQ_1	3rd adjust request value. Refer to [15:0] of 0x0910 for bit field detail

0x0914	LT_CONFIG_5	RW
POD: 0xF0F0A5A5		
BIT	**BIT NAME**	**FUNCTION**
15:0	ADJ_REQ_2	4th adjust request value. Refer to [15:0] of 0x0910 for bit field detail
31:16	ADJ_REQ_3	5th adjust request value. Refer to [15:0] of 0x0910 for bit field detail

0x0918	LT_CONFIG_6	RW
POD: 0x5A5A5555		
BIT	**BIT NAME**	**FUNCTION**
15:0	ADJ_REQ_4	6th adjust request value. Refer to [15:0] of 0x0910 for bit field detail
31:16	ADJ_REQ_5	7th adjust request value. Refer to [15:0] of 0x0910 for bit field detail

0x091C	LT_CONFIG_7	RW
POD: 0xF0F0A5A5		
BIT	**BIT NAME**	**FUNCTION**
15:0	ADJ_REQ_6	8th adjust request value. Refer to [15:0] of 0x0910 for bit field detail
31:16	ADJ_REQ_7	9th adjust request value. Refer to [15:0] of 0x0910 for bit field detail

0x0920	LT_CONFIG_8	RW
POD: 0x5A5A5555		
BIT	**BIT NAME**	**FUNCTION**
15:0	ADJ_REQ_8	10th adjust request value. Refer to [15:0] of 0x0910 for bit field detail
31:16	ADJ_REQ_9	11th adjust request value. Refer to [15:0] of 0x0910 for bit field detail

0x0924	LT_CONFIG_9	RW
POD: 0xF0F0A5A5		
BIT	**BIT NAME**	**FUNCTION**
15:0	ADJ_REQ_10	12th adjust request value. Refer to [15:0] of 0x0910 for bit field detail
31:16	ADJ_REQ_11	13th adjust request value. Refer to [15:0] of 0x0910 for bit field detail

0x0928	LT_CONFIG_A	RW
POD: 0x5A5A5555		
BIT	**BIT NAME**	**FUNCTION**
15:0	ADJ_REQ_12	14th adjust request value. Refer to [15:0] of 0x0910 for bit field detail
31:16	ADJ_REQ_13	15th adjust request value. Refer to [15:0] of 0x0910 for bit field detail

0x092C	LT_CONFIG_B	RW
POD: 0x0000A5A5		

BIT	BIT NAME	FUNCTION
15:0	ADJ_REQ_14	16th adjust request value. Refer to [15:0] of 0x0910 for bit field detail
31:16	ADJ_REQ_15	1st adjust request value. Refer to [15:0] of 0x0910 for bit field detail

3.3.6. DPCD_LTTPR_CAP_ID

0x0A00	DPCD_LTTPR_CAP_ID_0	RW
POD: 0x55801E14		
LT_DPCD MAX_LINK_RATE_PHY_RPTR (DPCD_ADDR F0000h-F0003)		

BIT	BIT NAME	FUNCTION
7:0	LT_TUNABLE_REV	DPCD LT_Tunable_phy_rptr_field_data_structure_rev (dpcd_addr=0xF0000 aux read only)
15:8	MAX_LINK_RATE	Maximum link rate of Main-Link Lanes = Value x 0.27Gbps (dpcd_addr=0xF0001 aux read only)
23:16	PHY_RPTR_CNT	Determine PHY_RPTR[8:1] (dpcd_addr=0xF0002)
31:24	PHY_RPTR_MODE	“55h” Transparent Mode, “AAh” Non-Transparent Mode (dpcd_addr=0xF0003)

0x0A04	DPCD_LTTPR_CAP_ID_1	RW
POD: 0x00000004		
DPCD address 0xF0004 MAX_LANE_COUNT_PHY_REPEATER		

BIT	BIT NAME	FUNCTION
4:0	MAX_LANE_COUNT	**MAX_LANE_COUNT** Only three values are supported. All other values are RESERVED. 1h = One lane (Lane 0 only). 2h = Two lanes (Lanes 0 and 1 only). 4h = Four lanes (Lanes 0, 1, 2, and 3).
31:5	Reserved	Reserved

3.3.7. DPCD_LTTPR_CONF_STATUS

0x0B00	DPCD_LTTPR_CONF_STATUS_13_10	RW
DPCD ADDR F0010h + 50h * REPEATER_CNT TRAINING_PATTERN_SELECT bits 7:0 DPCD ADDR F0011h + 50h * REPEATER_CNT TRAINING_LANE0_SET bits 15:8 DPCD ADDR F0012h + 50h * REPEATER_CNT TRAINING_LANE1_SET bits 23:16 DPCD ADDR F0013h + 50h * REPEATER_CNT TRAINING_LANE2_SET bits 31:24		

BIT	BIT NAME	FUNCTION
3:0	training_pattern_selection	**TRAINING_PATTERN_SET_PHY_REPEATER1** Link Training Pattern Selection. 0000 = Training not in progress (or disabled). 0001 = Link Training Pattern Sequence 1. 0010 = Link Training Pattern Sequence 2. 0011 = Link Training Pattern Sequence 3. 0111 = Link Training Pattern Sequence 4. All other values are RESERVED.
4	recovered_clock_out_en	0 = Recovered clock output from a test pad of DP RX is not enabled. 1 = Recovered clock output from a test pad of DP RX enabled.
5	scrambling_disable	0 = DPTX scrambles data symbols before transmission. 1 = DPTX disables scrambler and transmits all symbols without scrambling.
7:6	symbol_error_count_sel	00 = Count Disparity and Illegal Symbol errors 01 = Count Disparity errors only 10 = Count Illegal Symbol errors only 11 = RESERVED
9:8	voltage_swing_set_lane0	**TRAINING_LANE0_SET -VOLTAGE SWING SET** 00 = Voltage swing level 0. 01 = Voltage swing level 1. 10 = Voltage swing level 2. 11 = Voltage swing level 3.
10	max_swing_reached_lane0	**MAX_SWING_REACHED** The transmitter must support at least three levels of voltage swing (levels 0, 1 and 2). If only three levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 10 (level 2)), then this bit must be set to 1, and cleared in all other cases. If all four levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 11 (level 3)), then this bit must be set to 1,and cleared in all other cases.
12:11	pre_emphasis_set_lane0	**PRE-EMPHASIS_SET** 00 = Pre-emphasis level 0.

		01 = Pre-emphasis level 1. 10 = Pre-emphasis level 2. 11 = Pre-emphasis level 3.
13	max_pre_emphasis_reached_lane0	**MAX_PRE-EMPHASIS_REACHED** The transmitter must support at least three levels of pre-emphasis (levels 0, 1 and 2). Support of additional pre-emphasis level is optional. If only three levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10 (level 2)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. If all four levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11 (level 3)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. Support of independent pre-emphasis level control for each lane is also optional.
15:14	Reserved	**RESERVED**
17:16	voltage_swing_set_lane1	**TRAINING_LANE1_SET -VOLTAGE SWING SET** 00 = Voltage swing level 0. 01 = Voltage swing level 1. 10 = Voltage swing level 2. 11 = Voltage swing level 3.
18	max_swing_reached_lane1	**MAX_SWING_REACHED** The transmitter must support at least three levels of voltage swing (levels 0, 1 and 2). If only three levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 10 (level 2)), then this bit must be set to 1, and cleared in all other cases. If all four levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 11 (level 3)), then this bit must be set to 1,and cleared in all other cases.
20:19	pre_emphasis_set_lane1	**PRE-EMPHASIS_SET** 00 = Pre-emphasis level 0. 01 = Pre-emphasis level 1. 10 = Pre-emphasis level 2. 11 = Pre-emphasis level 3.
21	max_pre_emphasis_reached_lane1	**MAX_PRE-EMPHASIS_REACHED**

		The transmitter must support at least three levels of pre-emphasis (levels 0, 1 and 2). Support of additional pre-emphasis level is optional. If only three levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10 (level 2)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. If all four levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11 (level 3)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. Support of independent pre-emphasis level control for each lane is also optional.
23:22	Reserved	RESERVED
25:24	voltage_swing_set_lane2	**TRAINING_LANE1_SET -VOLTAGE SWING SET** 00 = Voltage swing level 0. 01 = Voltage swing level 1. 10 = Voltage swing level 2. 11 = Voltage swing level 3.
26	max_swing_reached_lane2	**MAX_SWING_REACHED** The transmitter must support at least three levels of voltage swing (levels 0, 1 and 2). If only three levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 10 (level 2)), then this bit must be set to 1, and cleared in all other cases. If all four levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 11 (level 3)), then this bit must be set to 1,and cleared in all other cases.
28:27	pre_emphasis_set_lane2	**PRE-EMPHASIS_SET** 00 = Pre-emphasis level 0. 01 = Pre-emphasis level 1. 10 = Pre-emphasis level 2. 11 = Pre-emphasis level 3.
29	max_pre_emphasis_reached_lane2	**MAX_PRE-EMPHASIS_REACHED** The transmitter must support at least three levels of pre-emphasis (levels 0, 1 and 2). Support of additional pre-emphasis level is optional. If only three levels of pre-emphasis are supported (transmitter programmed

		PRE-EMPHASIS_SET field (bits 4:3) to 10 (level 2)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. If all four levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11 (level 3)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. Support of independent pre-emphasis level control for each lane is also optional.
31:30	Reserved	RESERVED

0x0B04	DPCD_LTTPR_CONF_STATUS_17_14	RW
DPCD ADDR F0014h + 50h * REPEATER_CNT TRAINING_LANE3_SET bits 7:0 DPCD ADDR F0015h + 50h * REPEATER_CNT LINK_QUAL_LANE0_SET bits 15:8 DPCD ADDR F0016h + 50h * REPEATER_CNT LINK_QUAL_LANE1_SET bits 23:8 DPCD ADDR F0017h + 50h * REPEATER_CNT LINK_QUAL_LANE2_SET bits 31:24		
BIT	**BIT NAME**	**FUNCTION**
1:0	voltage_swing_set_lane3	TRAINING_LANE0_SET -VOLTAGE SWING SET 00 = Voltage swing level 0. 01 = Voltage swing level 1. 10 = Voltage swing level 2. 11 = Voltage swing level 3.
2	max_swing_reached_lane3	MAX_SWING_REACHED The transmitter must support at least three levels of voltage swing (levels 0, 1 and 2). If only three levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 10 (level 2)), then this bit must be set to 1, and cleared in all other cases. If all four levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 11 (level 3)), then this bit must be set to 1,and cleared in all other cases.
4:3	pre_emphasis_set_lane3	PRE-EMPHASIS_SET 00 = Pre-emphasis level 0. 01 = Pre-emphasis level 1. 10 = Pre-emphasis level 2. 11 = Pre-emphasis level 3.
5	max_pre_emphasis_reached_lane3	MAX_PRE-EMPHASIS_REACHED

		The transmitter must support at least three levels of pre-emphasis (levels 0, 1 and 2). Support of additional pre-emphasis level is optional. If only three levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10 (level 2)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. If all four levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11 (level 3)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. Support of independent pre-emphasis level control for each lane is also optional.
31:6	Reserved	RESERVED

0x0B08	**DPCD_LTTPR_CONF_STATUS_1B_18**	**RW**

DPCD ADDR F0018h + 50h * REPEATER_CNT **LINK_QUAL_LANE3_SET bits 7:0**

BIT	BIT NAME	FUNCTION
2:0	link_qual_pattern_set_lane3	**LINK_QUAL_LANE3_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect. The controls in this register supersede the controls in the TRAINING_PATTERN_SET register (DPCD Address 00102h). **LINK_QUAL_PATTERN_SET** 000 = Link quality test pattern not transmitted. 001 = D10.2 test pattern (unscrambled) transmitted (same as Link Training Pattern Sequence 1). 010 = Symbol Error Rate Measurement Pattern transmitted. 011 = PRBS7 transmitted. 100 = 80-bit custom pattern transmitted. 101 = CP2520 (HBR2 Compliance EYE pattern) transmitted. 110, 111 = RESERVED.
31:3	Reserved	RESERVED

0x0B10	DPCD_LTTPR_CONF_STATUS_23_20	RO

DPCD ADDR F0020h + 50h * REPEATER_CNT TRAINING_AUX_RD_INTERVAL_PHY Repeater1 bits 7:0
DPCD ADDR F0021h + 50h * REPEATER_CNT Transmitter Capability PHY Repeater1 bits 15:8

BIT	BIT NAME	FUNCTION
6:0	train_rd_interval	**TRAINING_AUX_RD_INTERVAL_PHY_REPEATER1** Bit definition is identical to that of the TRAINING_AUX_RD_INTERVAL register (DPCD Address 0220Eh).
7	Reserved	RESERVED
8	volt_swing_level_3	**VOLTAGE_SWING_LEVEL_3_SUPPORTED** 0 = Not supported. 1 = Supported.
9	pre_emp_level_3	**PRE_EMPHASIS_LEVEL_3_SUPPORTED** 0 = Not supported. 1 = Supported.
31:10	Reserved	RESERVED

0x0B20	DPCD_LTTPR_CONF_STATUS_33_30	RO

LT_DPCD_PHY_RPTR
DPCD ADDR F0030h + 50h * REPEATER_CNT LANE0_1_STATUS bits 7:0
DPCD ADDR F0031h + 50h * REPEATER_CNT LANE2_3_STATUS bits 15:8
DPCD ADDR F0032h + 50h * REPEATER_CNT LANE_ALIGN_STATUS bits 23;16
DPCD ADDR F0033h + 50h * REPEATER_CNT ADJUST_REQ_LANE0_1_STATUS bits 31:24

BIT	BIT NAME	FUNCTION
0	Lane0_cr_done	LANE0_CR_DONE (for AUX Read Only)
1	Lane0_eq_done	LANE0_EQ_DONE (for AUX Read Only)
2	Lane0_sym_locked	LANE0_SYM_LOCKED (for AUX Read Only)
3	Reserved	Reserved
4	Lane1_cr_done	LANE1_CR_DONE (for AUX Read Only)
5	Lane1_eq_done	LANE1_EQ_DONE (for AUX Read Only)
6	Lane1_sym_locked	LANE1_SYM_LOCKED (for AUX Read Only)
7	Reserved	Reserved
8	Lane2_cr_done	LANE2_CR_DONE (for AUX Read Only)
9	Lane2_eq_done	LANE2_EQ_DONE (for AUX Read Only)
10	Lane2_sym_locked	LANE2_SYM_LOCKED (for AUX Read Only)
11	Reserved	Reserved
12	Lane3_cr_done	LANE3_CR_DONE (for AUX Read Only)
13	Lane3_eq_done	LANE3_EQ_DONE (for AUX Read Only)
14	Lane3_sym_locked	LANE3_SYM_LOCKED (for AUX Read Only)
15	Reserved	Reserved
23:16	Lane_align_status_updated	LANE_ALIGN_STATUS_UPDATED
25:24	Volt_swing_lane0	**VOLT_SWING_LANE0** 00 = Level 0 01 = Level 1

		10 = Level 2 11 = Level 3
27:26	Pre_emp_lane0	**PRE_EMP_LANE0** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
29:28	Volt_swing_lane1	**VOLT_SWING_LANE1** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
31:30	Pre_emp_lane1	**PRE_EMP_LANE1** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3

0x0B24	**DPCD_LTTPR_CONF_STATUS_37_34**	**RO**
DPCD ADDR F0034h + 50h * REPEATER_CNT ADJUST_REQ_LANE2_3_STATUS bits 7:0 DPCD ADDR F0035h + 50h * REPEATER_CNT SYMBOL_ERROR_COUNT_LANE_L0 bits 15:8 DPCD ADDR F0036h + 50h * REPEATER_CNT SYMBOL_ERROR_COUNT_LANE_H0 bits 23:16 DPCD ADDR F0037h + 50h * REPEATER_CNT SYMBOL_ERROR_COUNT_LANE_L1 bits 31:24		
BIT	**BIT NAME**	**FUNCTION**
1:0	Volt_swing_lane2	**VOLT_SWING_LANE2** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
3:2	Pre_emp_lane2	PRE_EMP_LANE2 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
5:4	Volt_swing_lane3	**VOLT_SWING_LANE3** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
7:6	Pre_emp_lane3	PRE_EMP_LANE3 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3
15:8	Sym_error_cnt_lane0_l	SYM_ERROR_CNT_LANE0_L
22:16	Sym_error_cnt_lane0_h	SYM_ERROR_CNT_LANE0_H

23	Sym_error_cnt_lan0_v	SYM_ERROR_CNT_LANE0_VALID
31:24	Sym_error_cnt_lane1_l	SYM_ERROR_CNT_LANE1_L

0x0B28	DPCD_LTTPR_CONF_STATUS_3B_38	RO
DPCD ADDR F0038h + 50h * REPEATER_CNT SYMBOL_ERROR_COUNT_LANE_H1 bits 7:0 DPCD ADDR F0039h + 50h * REPEATER_CNT SYMBOL_ERROR_COUNT_LANE_L2 bits 15:8 DPCD ADDR F003Ah + 50h * REPEATER_CNT SYMBOL_ERROR_COUNT_LANE_H2 bits 23:16 DPCD ADDR F003Bh + 50h * REPEATER_CNT SYMBOL_ERROR_COUNT_LANE_L3 bits 31:24		
BIT	**BIT NAME**	**FUNCTION**
6:0	Sym_error_cnt_lane1_h	SYM_ERROR_CNT_LANE1_H
7	Sym_error_cnt_lan1_v	SYM_ERROR_CNT_LANE1_V
15:8	Sym_error_cnt_lane2_l	SYM_ERROR_CNT_LANE2_L
22:16	Sym_error_cnt_lane2_h	SYM_ERROR_CNT_LANE2_H
23	Sym_error_cnt_lan2_v	SYM_ERROR_CNT_LANE2_V
31:24	Sym_error_cnt_lane3_l	SYM_ERROR_CNT_LANE3_L

0x0B2C	DPCD_LTTPR_CONF_STATUS_3F_3C	RO
DPCD ADDR F003Ch + 50h * REPEATER_CNT SYMBOL_ERROR_COUNT_LANE_H3 bits 7:0 DPCD ADDR F003Dh + 50h * REPEATER_CNT IEEE_OUI_1 bits 15:8 DPCD ADDR F003Eh + 50h * REPEATER_CNT IEEE_OUI_2 bits 23:16 DPCD ADDR F003Fh + 50h * REPEATER_CNT IEEE_OUI_3 bits 31:24		
BIT	**BIT NAME**	**FUNCTION**
6:0	Sym_error_cnt_lane3_h	SYM_ERROR_CNT_LANE3_H
7	Sym_error_cnt_lan3_v	SYM_ERROR_CNT_LANE1_V
15:8	IEEE_OUT1	IEEE_OUT1
23:16	IEEE_OUT2	IEEE_OUT2
31:24	IEEE_OUT3	IEEE_OUT3

3.3.8. Receiver Configuration Registers

Addresses of the tables are offset from the base address of each receiver PHY address space.

START ADDRESS	REGISTER BANK
0x0100	All DP receiver
0x1E00	All USB receiver
0x1100	UFP USBRX
0x1200	UFP DPRX ML0
0x1300	UFP DPRX ML1
0x1400	UFP DPRX ML2
0x1500	UFP DPRX ML3
0x2000	DFP USBRX1
0x2100	DFP USBRX2

0x18	RX_CTLE_TERM_SB_CTRL	RW
POD: 0x00481000		

BIT	BIT NAME	FUNCTION
15:0	Reserved	Reserved
16	RX_CTLE_TERM_LO	Lower the single ended termination resistance from 50ohm to 40ohm
31:17	Reserved	Reserved

0x1C	RX_PGA_CTRL	RW
POD: 0x0000000		

BIT	BIT NAME	FUNCTION
7:0	Reserved	Reserved
9:8	RX_RBR_PGA	Gain tuning bit for PGA after the CTLE in RBR
10	RX_RBR_PGA_ATT	PGA attenuation enable bit for RBR
11	RX_RBR_PGA_OVR	0: Use auto gain calibration result 1: Use register value
13:12	RX_HBR_PGA	Gain tuning bit for PGA after the CTLE in HBR
14	RX_HBR_PGA_ATT	PGA attenuation enable bit for HBR
15	RX_HBR_PGA_OVR	0: Use auto gain calibration result 1: Use register value
17:16	RX_HBR2_PGA	Gain tuning bit for PGA after the CTLE in HBR2
18	RX_HBR2_PGA_ATT	PGA attenuation enable bit for HBR2
19	RX_HBR2_PGA_OVR	0: Use auto gain calibration result 1: Use register value
21:20	RX_HBR3_PGA	Gain tuning bit for PGA after the CTLE in HBR3
22	RX_HBR3_PGA_ATT	PGA attenuation enable bit for HBR3
23	RX_HBR3_PGA_OVR	0: Use auto gain calibration result 1: Use register value

25:24	RX_GEN1_PGA	Gain tuning bit for PGA after the CTLE in USB Gen1
26	RX_GEN1_PGA_ATT	PGA attenuation enable bit for USB Gen1
27	RX_GEN1_PGA_OVR	0: Use auto gain calibration result 1: Use register value
29:28	RX_GEN2_PGA	Gain tuning bit for PGA after the CTLE in USB Gen2
30	RX_GEN2_PGA_ATT	PGA attenuation enable bit for USB Gen2
31	RX_GEN2_PGA_OVR	0: Use auto gain calibration result 1: Use register value

0x24	RX_DFE_TAP_CTRL	RW
POD: 0x20202020		

BIT	BIT NAME	FUNCTION
5:0	RX_SUM_TAP1_SPI	Configurable control code to Summer TapDAC
7:6	Reserved	Reserved
13:8	RX_SUM_TAP2_SPI	Configurable control code to Summer TapDAC
15:14	Reserved	Reserved
21:16	RX_SUM_TAP3_SPI	Configurable control code to Summer TapDAC
23:22	Reserved	Reserved
29:24	RX_SUM_TAP4_SPI	Configurable control code to Summer TapDAC
31:30	Reserved	Reserved

0x28	RX_DFE_CTRL	RW
POD: 0x00202000		

BIT	BIT NAME	FUNCTION
0	Reserved	Reserved
1	RX_SUM_TAPWEIGHTSEL1	To enable configurable control of Summer Tap1 Weights
2	RX_SUM_TAPWEIGHTSEL2	To enable configurable control of Summer Tap2 Weights
3	RX_SUM_TAPWEIGHTSEL3	To enable configurable control of Summer Tap3 Weights
4	RX_SUM_TAPWEIGHTSEL4	To enable configurable control of Summer Tap4 Weights
31:5	Reserved	Reserved

0x70	RX_RBR_RX_Manual_EN	RW
POD: 0x25DF1460		

BIT	BIT NAME	FUNCTION
3:0	RBR_CTLE_CAP	1st EQ capacitance tuning bits. LSB change peak freq by ~10%. Default is 0
7:4	RBR_CTLE_ALGO	H1 + H2 is default for RBR
13:8	RBR_CTLE_RES	1st EQ degeneration resistance tuning bits. LSB changes boost by 0.5dB.

		ch1 (18dB) : 001010 ch2 (23dB) : 001110 ch3 (23dB) : 000101 ch4 (12dB) : 010001 (PGA should be 001) 42inch (25dB) : 011010 LMS value from adaptation engine is default.
14	RBR_CTLER_OVR	CTLE Setting Manual Setting Enable bit 0: Adaptation results for R 1: Referred to registers values
15	Reserved	Reserved
20:16	RBR_CLK_TUNE	Bandwidth control for waveform shaping. 00000: Maximum bandwidth 11111: Minimum bandwidth (Default)
23:21	RBR_PI_CLOAD	Cap load tuning for PI core outputs 000: USB Gen2, DP HBR3 010: USB Gen1, DP HBR2 100: DP HBR 110: DP RBR (Default)
26:24	RBR_CDR_IGAIN	CDR GAIN for Integral path 5: default for RBR
27	Reserved	Reserved
29:28	RBR_CDR_PGAIN	CDR GAIN for Proportional path 2: default for RBR
31:30	Reserved	Reserved

0x74	**RX_HBR_RX_Manual_EN**	**RW**
POD: 0x258F1460		
BIT	**BIT NAME**	**FUNCTION**
3:0	HBR_CTLE_CAP	1st EQ capacitance tuning bits. LSB change peak freq by ~10%. Default is 0
7:4	HBR_CTLE_ALGO	H1 + H2 is default for HBR
13:8	HBR_CTLE_RES	1st EQ degeneration resistance tuning bits. LSB changes boost by 0.5dB. ch1 (18dB) : 001010 ch2 (23dB) : 001110 ch3 (23dB) : 000101 ch4 (12dB) : 010001 (PGA should be 001) 42inch (25dB) : 011010 LMS value from adaptation engine is default.
14	HBR_CTLER_OVR	CTLE Setting Manual Setting Enable bit 0: Adaptation results for R 1: Referred to registers values
15	Reserved	Reserved
20:16	HBR_CLK_TUNE	Bandwidth control for waveform shaping. 00000: Maximum bandwidth 01111: Default for HBR

		11111: Minimum bandwidth
23:21	HBR_PI_CLOAD	Cap load tuning for PI core outputs 000: USB Gen2, DP HBR3 010: USB Gen1, DP HBR2 100: DP HBR (Default) 110: DP RBR
26:24	HBR_CDR_IGAIN	CDR GAIN for Integral path 5: default for HBR
27	Reserved	Reserved
29:28	HBR_CDR_PGAIN	CDR GAIN for Proportional path 2: default for HBR
31:30	Reserved	Reserved

0x78	**RX_HBR2_RX_Manual_EN**	**RW**
POD: 0x13471460		
BIT	**BIT NAME**	**FUNCTION**
3:0	HBR2_CTLE_CAP	1st EQ capacitance tuning bits. LSB change peak freq by ~10%. Default is 0
7:4	HBR2_CTLE_ALGO	H1 + H2 is default for HBR2
13:8	HBR2_CTLE_RES	1st EQ degeneration resistance tuning bits. LSB changes boost by 0.5dB. ch1 (18dB) : 001010 ch2 (23dB) : 001110 ch3 (23dB) : 000101 ch4 (12dB) : 010001 (PGA should be 001) 42inch (25dB) : 011010 LMS value from adaptation engine is default.
14	HBR2_CTLER_OVR	CTLE Setting Manual Setting Enable bit 0: Adaptation results for R 1: Referred to registers values
15	Reserved	Reserved
20:16	HBR2_CLK_TUNE	Bandwidth control for waveform shaping. 00000: Maximum bandwidth 00111: Default for HBR2 11111: Minimum bandwidth
23:21	HBR2_PI_CLOAD	Cap load tuning for PI core outputs 000: USB Gen2, DP HBR3 010: USB Gen1, DP HBR2 (Default) 100: DP HBR 110: DP RBR
26:24	HBR2_CDR_IGAIN	CDR GAIN for Integral path 3: default for HBR2
27	Reserved	Reserved
29:28	HBR2_CDR_PGAIN	CDR GAIN for Proportional path 1: default for HBR2

31:30	Reserved	Reserved

0x7C	RX_HBR3_RX_Manual_EN	RW
POD: 0x14001488		

BIT	BIT NAME	FUNCTION
3:0	HBR3_CTLE_CAP	1st EQ capacitance tuning bits. LSB change peak freq by ~10%. Default is 8
7:4	HBR3_CTLE_ALGO	H2 is default for HBR3
13:8	HBR3_CTLE_RES	1st EQ degeneration resistance tuning bits. LSB changes boost by 0.5dB. ch1 (18dB) : 001010 ch2 (23dB) : 001110 ch3 (23dB) : 000101 ch4 (12dB) : 010001 (PGA should be 001) 42inch (25dB) : 011010 LMS value from adaptation engine is default.
14	HBR3_CTLER_OVR	CTLE Setting Manual Setting Enable bit 0: Adaptation results for R 1: Referred to registers values
15	Reserved	Reserved
20:16	HBR3_CLK_TUNE	Bandwidth control for waveform shaping. 00000: Maximum bandwidth (Default) 11111: Minimum bandwidth
23:21	HBR3_PI_CLOAD	Cap load tuning for PI core outputs 000: USB Gen2, DP HBR3 (Default) 010: USB Gen1, DP HBR2 100: DP HBR 110: DP RBR
26:24	HBR3_CDR_IGAIN	CDR GAIN for Integral path 4: default for HBR3
27	Reserved	Reserved
29:28	HBR3_CDR_PGAIN	CDR GAIN for Proportional path 1: default for HBR3
31:30	Reserved	Reserved

0x80	RX_Gen1_RX_Manual_EN	RW
POD: 0x14471460		

BIT	BIT NAME	FUNCTION
3:0	GEN1_CTLE_CAP	1st EQ capacitance tuning bits. LSB change peak freq by ~10%. Default is 0
7:4	GEN1_CTLE_ALGO	H1+H2 is default for GEN1
13:8	GEN1_CTLE_RES	1st EQ degeneration resistance tuning bits. LSB changes boost by 0.5dB. ch1 (18dB) : 001010

		ch2 (23dB) : 001110 ch3 (23dB) : 000101 ch4 (12dB) : 010001 (PGA should be 001) 42inch (25dB) : 011010 LMS value from adaptation engine is default.
14	GEN1_CTLER_OVR	CTLE Setting Manual Setting Enable bit 0: Adaptation results for R 1: Referred to registers values
15	Reserved	Reserved
20:16	GEN1_CLK_TUNE	Bandwidth control for waveform shaping. 00000: Maximum bandwidth 00111: Default for Gen1 (Default) 11111: Minimum bandwidth
23:21	GEN1_PI_CLOAD	Cap load tuning for PI core outputs 000: USB Gen2, DP HBR3 010: USB Gen1, DP HBR2 (Default) 100: DP HBR 110: DP RBR
26:24	GEN1_CDR_IGAIN	CDR GAIN for Integral path 4: default for Gen1
27	Reserved	Reserved
29:28	GEN1_CDR_PGAIN	CDR GAIN for Proportional path 0: default for Gen1
31:30	Reserved	Reserved

0x84	**RX_Gen2_RX_Manual_EN**	**RW**
POD: 0x14001408		
BIT	**BIT NAME**	**FUNCTION**
3:0	GEN2_CTLE_CAP	1st EQ capacitance tuning bits. LSB change peak freq by ~10%. Default is 8
7:4	GEN2_CTLE_ALGO	H5+H6+H7 is default for GEN2
13:8	GEN2_CTLE_RES	1st EQ degeneration resistance tuning bits. LSB changes boost by 0.5dB. ch1 (18dB) : 001010 ch2 (23dB) : 001110 ch3 (23dB) : 000101 ch4 (12dB) : 010001 (PGA should be 001) 42inch (25dB) : 011010 LMS value from adaptation engine is default.
14	GEN2_CTLER_OVR	CTLE Setting Manual Setting Enable bit 0: Adaptation results for R 1: Referred to registers values
15	Reserved	Reserved
20:16	GEN2_CLK_TUNE	Bandwidth control for waveform shaping. 00000: Maximum bandwidth (Default) 11111: Minimum bandwidth

23:21	GEN2_PI_CLOAD	Cap load tuning for PI core outputs 000: USB Gen2, DP HBR3 (Default) 010: USB Gen1, DP HBR2 100: DP HBR 110: DP RBR
26:24	GEN2_CDR_IGAIN	CDR GAIN for Integral path 4: default for Gen2
27	Reserved	Reserved
29:28	GEN2_CDR_PGAIN	CDR GAIN for Proportional path 0: default for Gen2
31:30	Reserved	Reserved

0x88	**RX_DFE_ADAPT_CTRL**	**RW**
POD: 0xCD222222		
BIT	**BIT NAME**	**FUNCTION**
2:0	RBR_EQ_MODE_TAP	LMS counter depth (1/u) setting for TAP 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) (Default) [others: MSB=18 (u=2^-18)]
3	Reserved	Reserved
6:4	HBR_EQ_MODE_TAP	LMS counter depth (1/u) setting for TAP 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) (Default) [others: MSB=18 (u=2^-18)]
7	Reserved	Reserved
10:8	HBR2_EQ_MODE_TAP	LMS counter depth (1/u) setting for TAP 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) (Default) [others: MSB=18 (u=2^-18)]
11	Reserved	Reserved
14:12	HBR3_EQ_MODE_TAP	LMS counter depth (1/u) setting for TAP 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12)

		011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) (Default) [others: MSB=18 (u=2^-18)]
15	Reserved	Reserved
18:16	GEN1_EQ_MODE_TAP	LMS counter depth (1/u) setting for TAP 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) (Default) [others: MSB=18 (u=2^-18)]
19	Reserved	Reserved
22:20	GEN2_EQ_MODE_TAP	LMS counter depth (1/u) setting for TAP 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) (Default) [others: MSB=18 (u=2^-18)]
23	Reserved	Reserved
27:24	GEN1_EQ_WAIT_TAP	Wait time for DFE LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
31:28	GEN2_EQ_WAIT_TAP	Wait time for DFE LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.

0x8C	**RX_CTLE_ADAPT_MODE**	**RW**
POD: 0xC9111111		
BIT	**BIT NAME**	**FUNCTION**
2:0	RBR_EQ_MODE_CTLE	LMS counter depth (1/u) setting for CTLE 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) (Default) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
3	Reserved	Reserved
6:4	HBR_EQ_MODE_CTLE	LMS counter depth (1/u) setting for CTLE 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) (Default) 100: MSB=16 (u=2^-16)

		101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
7	Reserved	Reserved
10:8	HBR2_EQ_MODE_CTLE	LMS counter depth (1/u) setting for CTLE 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) (Default) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
11	Reserved	Reserved
14:12	HBR3_EQ_MODE_CTLE	LMS counter depth (1/u) setting for CTLE 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) (Default) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
15	Reserved	Reserved
18:16	GEN1_EQ_MODE_CTLE	LMS counter depth (1/u) setting for CTLE 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) (Default) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
19	Reserved	Reserved
22:20	GEN2_EQ_MODE_CTLE	LMS counter depth (1/u) setting for CTLE 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) 011: MSB=14 (u=2^-14) (Default) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
23	Reserved	Reserved
27:24	GEN1_EQ_WAIT_CTLE	Wait time for CTLE LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
31:28	GEN2_EQ_WAIT_CTLE	Wait time for CTLE LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.

0x90	RX_THR_ADAPT_MODE	RW
POD: 0x45000000		

BIT	BIT NAME	FUNCTION
2:0	RBR_EQ_MODE_THR	LMS counter depth (1/u) setting for THR 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) (Default) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
3	Reserved	Reserved
6:4	HBR_EQ_MODE_THR	LMS counter depth (1/u) setting for THR 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) (Default) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
7	Reserved	Reserved
10:8	HBR2_EQ_MODE_THR	LMS counter depth (1/u) setting for THR 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) (Default) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
11	Reserved	Reserved
14:12	HBR3_EQ_MODE_THR	LMS counter depth (1/u) setting for THR 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) (Default) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
15	Reserved	Reserved
18:16	GEN1_EQ_MODE_THR	LMS counter depth (1/u) setting for THR 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) (Default) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
19	Reserved	Reserved

22:20	GEN2_EQ_MODE_THR	LMS counter depth (1/u) setting for THR 000: MSB=8 (u=2^-8) 001: MSB=10 (u=2^-10) 010: MSB=12 (u=2^-12) (Default) 011: MSB=14 (u=2^-14) 100: MSB=16 (u=2^-16) 101: MSB=18 (u=2^-18) [others: MSB=18 (u=2^-18)]
23	Reserved	Reserved
27:24	GEN1_EQ_WAIT_THR	Wait time for threshold LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
31:28	GEN2_EQ_WAIT_THR	Wait time for threshold LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.

0xA0	RX_EQ_ADAPT_WAIT0	RW
POD: 0xC8884444		
Receiver PHY manual configuration registers		

BIT	BIT NAME	FUNCTION
3:0	RBR_EQ_WAIT_THR	Wait time for THR LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
7:4	HBR_EQ_WAIT_THR	Wait time for THR LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
11:8	HBR2_EQ_WAIT_THR	Wait time for THR LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
15:12	HBR3_EQ_WAIT_THR	Wait time for THR LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
19:16	RBR_EQ_WAIT_CTLE	Wait time for CTLE LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
23:20	HBR_EQ_WAIT_CTLE	Wait time for CTLE LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
27:24	HBR2_EQ_WAIT_CTLE	Wait time for CTLE LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
31:28	HBR3_EQ_WAIT_CTLE	Wait time for CTLE LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.

0xA4	RX_EQ_ATAPT_WAIT1	RW
POD: 0x0000CCCC		

BIT	BIT NAME	FUNCTION
3:0	RBR_EQ_WAIT_TAP	Wait time for TAP LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
7:4	HBR_EQ_WAIT_TAP	Wait time for TAP LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.

11:8	HBR2_EQ_WAIT_TAP	Wait time for TAP LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
15:12	HBR3_EQ_WAIT_TAP	Wait time for TAP LMS in sequential EQ adaptation. 16384 x 2^(N/2) count in div32 clock.
31:16	Reserved	Reserved

0xB4	RX_PHYD_CTRL0	RW
POD: 0x008009C0		

BIT	BIT NAME	FUNCTION
5:0	RX_CTLE_RES_MIN0	CTLER minimum clamp setting for DFE disable
11:6	RX_CTLE_RES_MAX0	CTLER maximum clamp setting for DFE disable (default 39 decimal)
17:12	RX_CTLE_RES_MIN1	CTLER minimum clamp setting for DFE enable
23:18	RX_CTLE_RES_MAX1	CTLER maximum clamp setting for DFE enable (default 28 decimal)
24	Reserved	Reserved
28:25	AdaptCodeMuxSel	SS_ACODE monitor select
31:29	Reserved	Reserved

0xC0	RX_PHYD_MISC_CNTRL0	RW
POD: 0x2800AC1C		

BIT	BIT NAME	FUNCTION
23:0	EQ_ADAPT_CTRL	EQ Adaptation control register
24	RBR_DFE_ADAPT_EN	Enable bit for DFE adaptation in RBR 0: Disable (Default) 1: Enable
25	HBR_DFE_ADAPT_EN	Enable bit for DFE adaptation in HBR 0: Disable (Default) 1: Enable
26	HBR2_DFE_ADAPT_EN	Enable bit for DFE adaptation in HBR2 0: Disable (Default) 1: Enable
27	HBR3_DFE_ADAPT_EN	Enable bit for DFE adaptation in HBR3 0: Disable 1: Enable (Default)
28	GEN1_DFE_ADAPT_EN	Enable bit for DFE adaptation in USB Gen1 0: Disable (Default) 1: Enable
29	GEN2_DFE_ADAPT_EN	Enable bit for DFE adaptation in USB Gen2 0: Disable 1: Enable (Default)
31:30	Reserved	Reserved

0xD8	RX_CDR_RESET_CTRL	RW
POD: 0x00000601		

BIT	BIT NAME	FUNCTION
0	CDR_RESET_MODE	0: CDR reset duration is determined by [12:8] bits of this register 1: CDR reset duration during CR phase is 40-ns as same as C0 revision
7:1	RESERVED	
12:8	CDR_RESET_DURATION	Pulse width of CDR reset before CR phase. Reset duration is 40ns x CDR_RESET_DURATION when CDR_RESET_MODE = 0 Pulse width of PHY Front-end FIFO reset before starting CR phase
31:13	RESERVED	

3.3.9. Receiver Equalizer Status Monitoring Register

Addresses of the tables are offset from the base address of each receiver PHY address space.

START ADDRESS	REGISTER BANK
0x1100	UFP USBRX
0x1200	UFP DPRX ML0
0x1300	UFP DPRX ML1
0x1400	UFP DPRX ML2
0x1500	UFP DPRX ML3
0x2000	DFP USBRX1
0x2100	DFP USBRX2

0x94	RX_ADAPT_MONITOR0	RO
BIT	**BIT NAME**	**FUNCTION**
8:0	Reserved	
11:9	RX_SUMMER_EBTUNE_CAL	The Summer current code setting after Rx EQ adaptation
14:12	RX_ODAC_IBTUNE_CAL	The offset DAC bias current code after Rx offset calibration
15	RX_SUMMER_ATT_EN_CAL	The CTLE attenuation after Rx EQ adaptation
18:16	RX_THRESH_IBTUNE_CAL	The Threshold DAC current code after Rx EQ adaptation
19	Reserved	
21:20	RX_CTLE_PGA_CAL	The CTLE PGA code after Rx EQ adaptation
23:22	GM_CTLE_CAL	The CTLE bias setting after Rx EQ adaptation
24	Reserved	
27:25	RX_TDAC_EBTUNE_CAL	The DFE Tap DAC current code after Rx EQ adaptation
30:28	RX_TAP1_EBTUNE_CAL	The 1st post cursor DFE Tap DAC current code after Rx EQ adaptation

31	Reserved	Reserved

0xB4	RX_CTLE_ADAPT_CONF	RW
POD: 0x008009C0		

BIT	BIT NAME	FUNCTION
5:0	RX_CTLE_RES_MIN0	CTLER minimum clamp setting for DFE disable
11:6	RX_CTLE_RES_MAX0	CTLER maximum clamp setting for DFE disable (default 39 decimal)
17:12	RX_CTLE_RES_MIN1	CTLER minimum clamp setting for DFE enable
23:18	RX_CTLE_RES_MAX1	CTLER maximum clamp setting for DFE enable (default 28 decimal)
24	Reserved	Reserved
28:25	AdaptCodeMuxSel	SS_ACODE monitor select
31:29	Reserved	Reserved

0xBC	RX_ADAPT_MONITOR1	RO

BIT	BIT NAME	FUNCTION
5:0	RX_SLICER_THE_LMS	Threshold LMS result
11:6	RX_SLICER_THO_LMS	Threshold LMS result
15:12	Reserved	Reserved
21:16	SS_ACODE	Bus to allow monitoring of various internal LMS/Offset adaptation codes. Selected by AdaptCodeMuxSel AdaptCodeMuxSel=4'h0 {2'b0, oPRE_EMPH_TOO_LO, oPRE_EMPH_TOO_HI, oVOL_SWING_TOO_LO, oVOL_SWING_TOO_HI} AdaptCodeMuxSel=4'h1 RX_SLICER_THE_LMS AdaptCodeMuxSel=4'h2 RX_SLICER_THO_LMS AdaptCodeMuxSel=4'h3 RX_SUM_TAP1_LMS AdaptCodeMuxSel=4'h4 RX_SUM_TAP2_LMS AdaptCodeMuxSel=4'h5 RX_SUM_TAP3_LMS AdaptCodeMuxSel=4'h6 RX_SUM_TAP4_LMS AdaptCodeMuxSel=4'h7 RX_CTLE_RES_LMS AdaptCodeMuxSel=4'h8 {2'h0,RX_CTLE_CAP_LMS} AdaptCodeMuxSel=4'h9 RX_OFFSET_CAL_DATA_EVEN AdaptCodeMuxSel=4'hA RX_OFFSET_CAL_DATA_ODD AdaptCodeMuxSel=4'hB RX_OFFSET_CAL_EDGE_EVEN AdaptCodeMuxSel=4'hC RX_OFFSET_CAL_EDGE_ODD AdaptCodeMuxSel=4'hD RX_OFFSET_CAL_TH_EVEN AdaptCodeMuxSel=4'hE RX_OFFSET_CAL_TH_ODD AdaptCodeMuxSel=4'hF {3'b0, SWING_LEVEL}
27:22	RX_CTLE_RES_LMS	CTLE adaptation result
31:28	Reserved	Reserved

0xE4	RX_ADAPT_MONITOR2	RO
BIT	**BIT NAME**	**FUNCTION**
5:0	RX_SUM_TAP1_LMS	DFE adaptation result for TAP1
11:6	RX_SUM_TAP2_LMS	DFE adaptation result for TAP2
17:12	RX_SUM_TAP3_LMS	DFE adaptation result for TAP3
23:18	RX_SUM_TAP4_LMS	DFE adaptation result for TAP4
31:24	Reserved	Reserved

3.3.10. Eye Opening Monitor Registers

Addresses of the tables are offset from the base address of each receiver PHY address space.

START ADDRESS	REGISTER BANK
0x1200	UFP DPRX ML0
0x1300	UFP DPRX ML1
0x1400	UFP DPRX ML2
0x1500	UFP DPRX ML3
0x0100	ALL DPRX (Write Only)
0x1100	UFP USBRX
0x2000	DFP USBRX1
0x2100	DFP USBRX2
0x1E00	ALL USB RX (Write Only)

0x50	RXPHY_CTRL0	RW
POD: 0x00005E80		
BIT	**BIT NAME**	**FUNCTION**
0	RX_RST	Reset all DP receivers 1: Reset assertion 0: Reset deassertion
1	RX_INVERT	Invert RX_RECDATA[31:0]. 0: Normal data 1: Inverted data
3:2	RX_SWAP	Bit order swap of RX_RECDATA[31:0]. 0: No swap (IN[31:0]) 1: {24'h0,IN[0:7]} 2: {16'h0,IN[0:15]} 3: IN[0:31]
5:4	RX_SWAP_ERR	Bit order swap for EOM data
6	RX_INVERT_ERR	Invert option for EOM data

10:7	Reserved	Reserved
11	RSTZ_EOM	Active low reset for EOM
31:12	Reserved	Reserved

0x54	RX_EOM_ACCUM_INTERVAL	RW
BIT	**BIT NAME**	**FUNCTION**
31:0	ERDD_BER_TH_XG	sets BER accumulation window

0x58	RX_EOM_START_VAL	RW
POD: 0x00007B20		
BIT	**BIT NAME**	**FUNCTION**
5:0	EOM_THR_INIT	Initial value for EOM vertical DAC
7:6	Reserved	Reserved
14:8	EOM_PHOS_INIT	Initial value for EOM horizontal phase code offset
31:15	Reserved	Reserved

0xB8	RX_EOM_CTRL	RW
POD: 0x10180000		
BIT	**BIT NAME**	**FUNCTION**
0	EOM_EN	EOM enable
1	EOM_START	EOM start
4:2	EOM_MODE	EOM mode 0: PRBS checker ERD is used 1: Live traffic check. Compare the output from data slicer and error slicer; D(n) ^ E(n) 2: Live traffic check. Compare the output from data slicer and error slicer with +/-1bit shift allowed; best result of D(n) ^ E(n), D(n) ^ E(n+1), and D(n) ^ E(n-1)
6:5	Reserved	Reserved
7	EQ_ADAPT_STOP	0: EQ adaptation logic is controlled by the hardware 1: EQ adaptation is forced to be stopped during eye scan.
31:8	Reserved	Reserved

0xC8	RX_PHYD_EOM_DAT	RO
POD: 0x00000000		
BIT	**BIT NAME**	**FUNCTION**
4:0	Reserved	
5	EOM_DONE	EOM done signal

11:6	EOM_THRMAX	EOM max vertical code
17:12	EOM_THRMIN	EOM min vertical code
24:18	EOM_PHOSMAX	EOM max horizontal code
31:25	EOM_PHOSMIN	EOM min horizontal code

0xD4	RX_EOM_CONFIG	RW
POD: 0x00440008		
BIT	**BIT NAME**	**FUNCTION**
16:0	EOM_EYELIM	EOM bit error limit
19:17	EOM_HSTEP	EOM horizontal step
22:20	EOM_VSTEP	EOM vertical step
23	EOM_OVR	EOM override
24	ERDE_EN_OVR	EOM ERD enable override
25	ERDE_RSLT_CLR_OVR	EOM ERD result clear override
31:26	Reserved	Reserved

3.3.11. Transmitter Configuration Registers

Addresses of the tables are offset from the base address of each transmitter PHY address space.

START ADDRESS	REGISTER BANK
0x2200	DFP DPTX ML3
0x2300	DFP DPTX ML0
0x2400	DFP DPTX ML2
0x2500	DFP DPTX ML1
0x0200	All DPTX (Write Only)
0x1000	UFP USB TX
0x2400	DFP USB TX1
0x2500	DFP USB TX2
0x1F00	All USBTX (Write Only)

0x40	TXPHY_CTRL0	RW
POD: 0x00000400		
BIT	**BIT NAME**	**FUNCTION**
0	TX_SOFT_RESET	Software reset for Tx logic. Active high.
7:1	Reserved	Reserved
8	TX_INVERT	Invert TX_DATAIN [31:0]. 0: Normal data 1: Inverted data

9	Reserved	Reserved
10	FIFO_AUTO_RESET_EN	TX FIFO auto reset enable. When high, fifo will be normal function mode.
31:9	Reserved	Reserved

0x4C	TX_GC_CTRL1	RW
POD: 0x8AA81A50		

BIT	BIT NAME	FUNCTION
2:0	Reserved	
6:3	TXGC_GAIN_USBGEN1	4-bits Phase code filter gain setting.
15:7	Reserved	
19:16	TX_GC_GAIN_RBR	4-bits Phase code filter gain setting.
23:20	TX_GC_GAIN_HBR	4-bits Phase code filter gain setting.
27:24	TX_GC_GAIN_HBR2	4-bits Phase code filter gain setting.
31:28	TX_GC_GAIN_HBR3	4-bits Phase code filter gain setting.

0x54	TX_CONF_WINDOW_0	RW
POD: 0x00000000		

BIT	BIT NAME	FUNCTION
4:0	TX_VML_SWING_EN	Configure Tx settings by using TX_CONF_CTRL
7:5	Reserved	Reserved
12:8	TX_VML_MAIN_EN	Configure Tx settings by using TX_CONF_CTRL
15:13	Reserved	Reserved
18:16	TX_VML_PRE_EN	Configure Tx settings by using TX_CONF_CTRL
19	Reserved	Reserved
23:20	TX_VML_POST_EN	Configure Tx settings by using TX_CONF_CTRL
26:24	TX_VML_PRE	Configure Tx settings by using TX_CONF_CTRL
27	Reserved	Reserved
31:28	TX_VML_POST	Configure Tx settings by using TX_CONF_CTRL

0x58	TX_CONF_WINDOW_1	RW
POD: 0x00000000		

BIT	BIT NAME	FUNCTION
0	TX_P2S_OUTP_HIGH_EN	Configure Tx settings by using TX_CONF_CTRL

1	TX_P2S_OUTN_HIGH_EN	Configure Tx settings by using TX_CONF_CTRL
2	TX_P2S_TEST_EN	Configure Tx settings by using TX_CONF_CTRL
3	TX_P2S_ACTIVE_EN	Configure Tx settings by using TX_CONF_CTRL
4	TX_P2S_PRE_PD	Configure Tx settings by using TX_CONF_CTRL
5	TX_P2S_POST_PD	Configure Tx settings by using TX_CONF_CTRL
6	TX_DYNAMIC_COMP_EN	Configure Tx settings by using TX_CONF_CTRL
7	Reserved	Reserved
12:8	TX_DYNAMIC_COMP_TUNE	Configure Tx settings by using TX_CONF_CTRL
15:13	TX_DLDO_TUNE	Configure Tx settings by using TX_CONF_CTRL
17:16	TX_CAL_SWING_MODE	Configure Tx settings by using TX_CONF_CTRL
19:18	TX_CLK_SEL	Configure Tx settings by using TX_CONF_CTRL
24:20	TX_CLK_TUNE	Configure Tx settings by using TX_CONF_CTRL
27:25	Reserved	Reserved
30:28	TX_PI_CLOAD	Configure Tx settings by using TX_CONF_CTRL
31	Reserved	Reserved

0x5C	**TX_CONF_CTRL**	**RW**
POD: 0x00000000		
BIT	**BIT NAME**	**FUNCTION**
4:0	CONF_SEL	0: USB Gen1 1: USB Gen2 2: USB LFPS 3: USB EI in P2 4: USB EI in P1 and P0 5: USB Gen1 LP 6: USB Gen2 LP 7: USB LFPS LP X: DP[(X-8)/4][(Xmod4)] [(X-8)/4]: Amplitude Level [(Xmod4)]: Pre-emphasis Level Where 8<=X<=23 28: DP RBR for WINDOW_1 29: DP HBR for WINDOW_1 30: DP HBR2 for WINDOW_1 31: DP HBR 3for WINDOW_1
6:5	Reserved	
7	RD_WR_SEL	0: Read 1: Write
31:8	Reserved	

0x54	TX_CONF_MONITOR_0	RW
POD: 0x00000000		

BIT	BIT NAME	FUNCTION
4:0	TX_VML_SWING_EN	Configure Tx settings by using TX_CONF_CTRL
7:5	Reserved	Reserved
12:8	TX_VML_MAIN_EN	Configure Tx settings by using TX_CONF_CTRL
15:13	Reserved	Reserved
18:16	TX_VML_PRE_EN	Configure Tx settings by using TX_CONF_CTRL
19	Reserved	Reserved
23:20	TX_VML_POST_EN	Configure Tx settings by using TX_CONF_CTRL
26:24	TX_VML_PRE	Configure Tx settings by using TX_CONF_CTRL
27	Reserved	Reserved
31:28	TX_VML_POST	Configure Tx settings by using TX_CONF_CTRL

0x58	TX_CONF_MONITOR_1	RW
POD: 0x00000000		

BIT	BIT NAME	FUNCTION
0	TX_P2S_OUTP_HIGH_EN	Configure Tx settings by using TX_CONF_CTRL
1	TX_P2S_OUTN_HIGH_EN	Configure Tx settings by using TX_CONF_CTRL
2	TX_P2S_TEST_EN	Configure Tx settings by using TX_CONF_CTRL
3	TX_P2S_ACTIVE_EN	Configure Tx settings by using TX_CONF_CTRL
4	TX_P2S_PRE_PD	Configure Tx settings by using TX_CONF_CTRL
5	TX_P2S_POST_PD	Configure Tx settings by using TX_CONF_CTRL
6	TX_DYNAMIC_COMP_EN	Configure Tx settings by using TX_CONF_CTRL
7	Reserved	Reserved
12:8	TX_DYNAMIC_COMP_TUNE	Configure Tx settings by using TX_CONF_CTRL
15:13	TX_DLDO_TUNE	Configure Tx settings by using TX_CONF_CTRL
17:16	TX_CAL_SWING_MODE	Configure Tx settings by using TX_CONF_CTRL
19:18	TX_CLK_SEL	Configure Tx settings by using TX_CONF_CTRL
24:20	TX_CLK_TUNE	Configure Tx settings by using TX_CONF_CTRL
27:25	Reserved	Reserved
30:28	TX_PI_CLOAD	Configure Tx settings by using TX_CONF_CTRL
31	Reserved	Reserved

4. Revision history

Table 2. Document revision history

Revision	Revision Date	Description	Remarks
1.0.0	June 28th, 2019	• Initial Release	

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