MOTOROLA

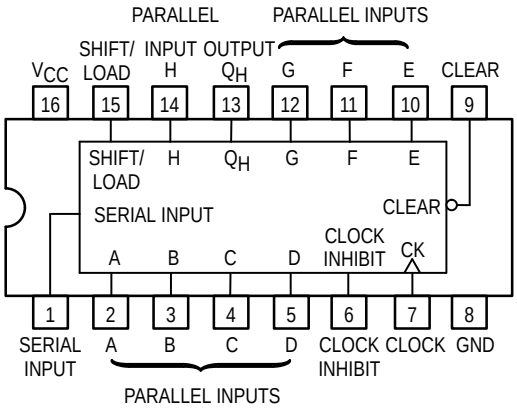
SN54/74LS166

8-BIT SHIFT REGISTERS

The SN54L/74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 54/74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

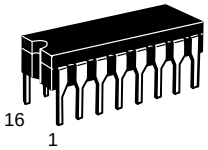
The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

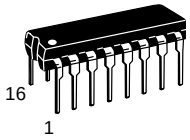


8-BIT SHIFT REGISTERS

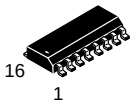
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

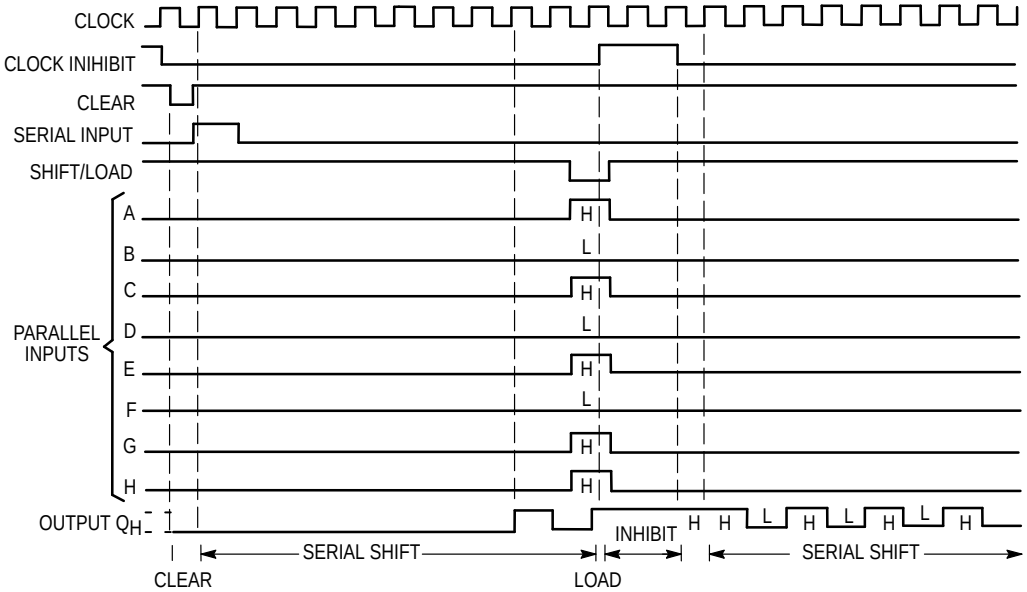
ORDERING INFORMATION

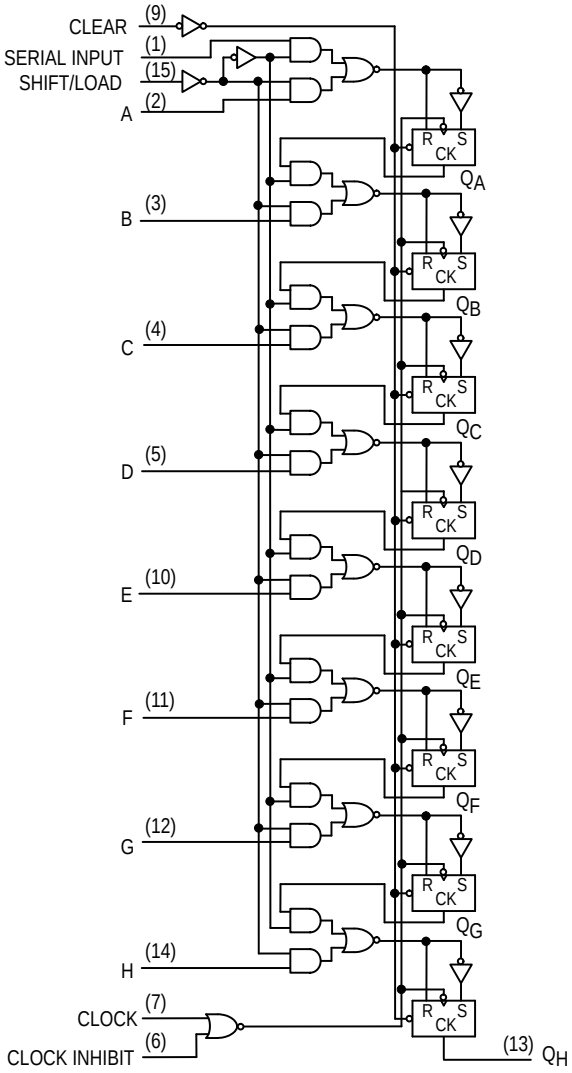
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT Q_H
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Typical Clear, Shift, Load, Inhibit, and Shift Sequences





GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

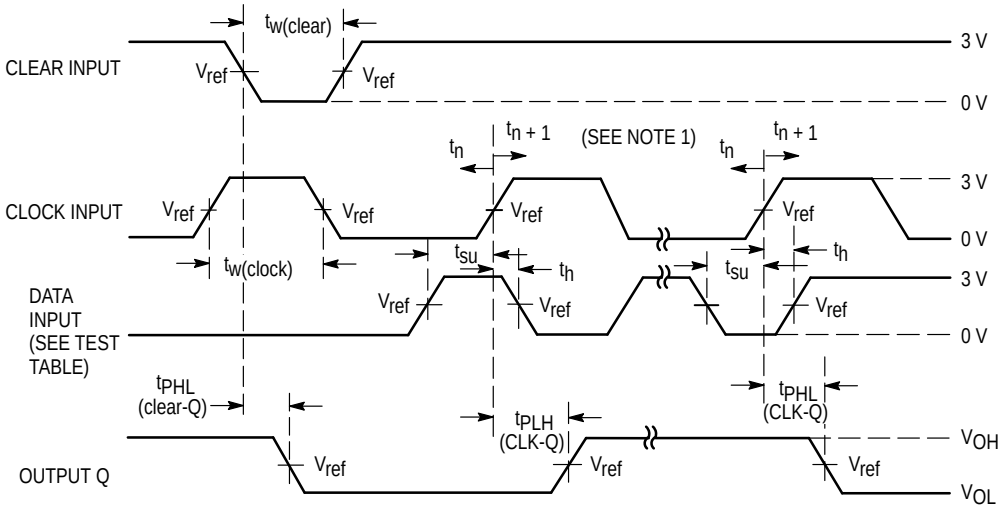
Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				38	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}

AC WAVEFORMS



NOTE 1. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transition
LS166 V_{ref} = 1.3 V.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	35		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Clear to Output		19	30	ns	
t_{PLH} t_{PHL}	Clock to Output		23 24	35 35	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_W	Clock Clear Pulse Width	30			ns	V_{CC} = 5.0 V
t_S	Mode Control Setup Time	30			ns	
t_S	Data Setup Time	20			ns	
t_h	Hold Time, Any Input	15			ns	