8-bit AVR Microcontroller

ATmega328PB

DATASHEET SUMMARY

Introduction

The Atmel® ATmega328PB is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega328PB achieves throughputs close to 1MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

Feature

High Performance, Low Power Atmel®AVR® 8-Bit Microcontroller Family

- Advanced RISC Architecture
  - 131 Powerful Instructions
  - Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 32KBytes of In-System Self-Programmable Flash program memory
  - 1KBytes EEPROM
  - 2KBytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C(1)
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- Peripheral Touch Controller
  - Capacitive touch buttons, sliders and wheels
  - 24 Self-cap channels and 144 mutual cap channels
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode

This is a summary document. A complete document is available on our Web site at www.atmel.com

  - Three 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Ten PWM Channels
  - 8-channel 10-bit ADC in TQFP and QFN/MLF package
  - Two Programmable Serial USART
  - Two Master/Slave SPI Serial Interface
  - Two Byte-oriented 2-wire Serial Interface (Philips I^2C compatible)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
  - Unique Device ID
- I/O and Packages
  - 27 Programmable I/O Lines
  - 32-pin TQFP and 32-pin QFN/MLF
- Operating Voltage:
  - 1.8 - 5.5V
- Temperature Range:
  - -40°C to 105°C
- Speed Grade:
  - 0 - 4MHz @ 1.8 - 5.5V
  - 0 - 10MHz @ 2.7 - 5.5.V
  - 0 - 20MHz @ 4.5 - 5.5V
- Power Consumption at 1MHz, 1.8V, 25°C
  - Active Mode: 0.2mA
  - Power-down Mode: 0.2µA
  - Power-save Mode: 1.3µA (Including 32kHz RTC)

Table of Contents

1. Description

The Atmel® ATmega328PB is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega328PB achieves throughputs close to 1MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

The Atmel AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in a single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega328PB provides the following features: 32Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 1Kbytes EEPROM, 2Kbytes SRAM, 27 general purpose I/O lines, 32 general purpose working registers, five flexible Timer/Counters with compare modes, internal and external interrupts, two serial programmable USART, two byte-oriented 2-wire Serial Interface (I2C), two SPI serial ports, a 8-channel 10-bit ADC in TQFP and QFN/MLF package, a programmable Watchdog Timer with internal Oscillator, Clock failure detection mechanism and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioning. PTC with enabling up to 24 self-cap and 144 mutual-cap sensors. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. Also ability to run PTC in power-save mode/wake-up on touch and Dynamic on/off of PTC analog and digital portion. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer, PTC, and ADC to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Composer allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega328PB is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega328PB is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2. Configuration Summary

Features	ATmega328PB
Pin count	32
Flash (KB)	32
SRAM (KB)	2
EEPROM (KB)	1
General Purpose I/O pins	27
SPI	2
TWI (I^2C)	2
USART	2
ADC	10-bit 15ksps
ADC channels	8
AC propagation delay	400ns (Typical)
8-bit Timer/Counters	2
16-bit Timer/Counters	3
PWM channels	10
PTC	Available
Clock Failure Detector (CFD)	Available
Output Compare Modulator (OCM1C2)	Available

3. Ordering Information

Speed [MHz]	Power Supply [V]	Ordering Code[2]	Package[1]	Operational Range
20	1.8 - 5.5	ATmega328PB-AU ATmega328PB-AUR[3] ATmega328PB-MU ATmega328PB-MUR[3]	32A 32A 32MS1 32MS1	Industrial (-40°C to 85°C)
		ATmega328PB-AN ATmega328PB-ANR[3] ATmega328PB-MN ATmega328PB-MNR[3]	32A 32A 32MS1 32MS1	Industrial (-40°C to 105°C)

Note: 1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.

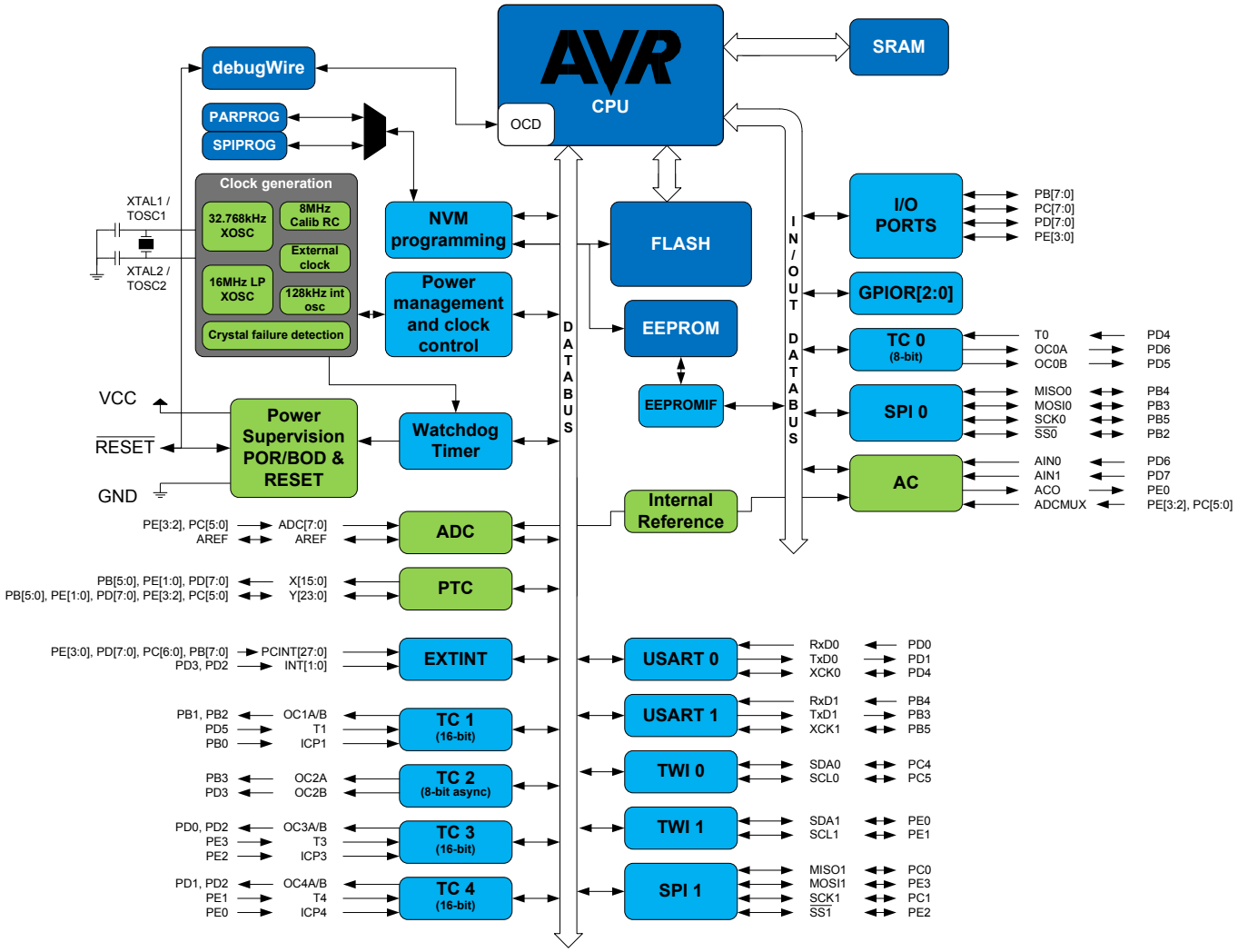
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. Tape & Reel.

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
32MS1	32-pad, 5.0x5.0x0.9mm body, Lead Pitch 0.50mm, Very-thin Fine pitch, Quad Flat No Lead Package (VQFN)

4. Block Diagram

Figure 4-1 Block Diagram



5. Pin Configurations

Figure 5-1 32 TQFP Pinout ATmega328PB

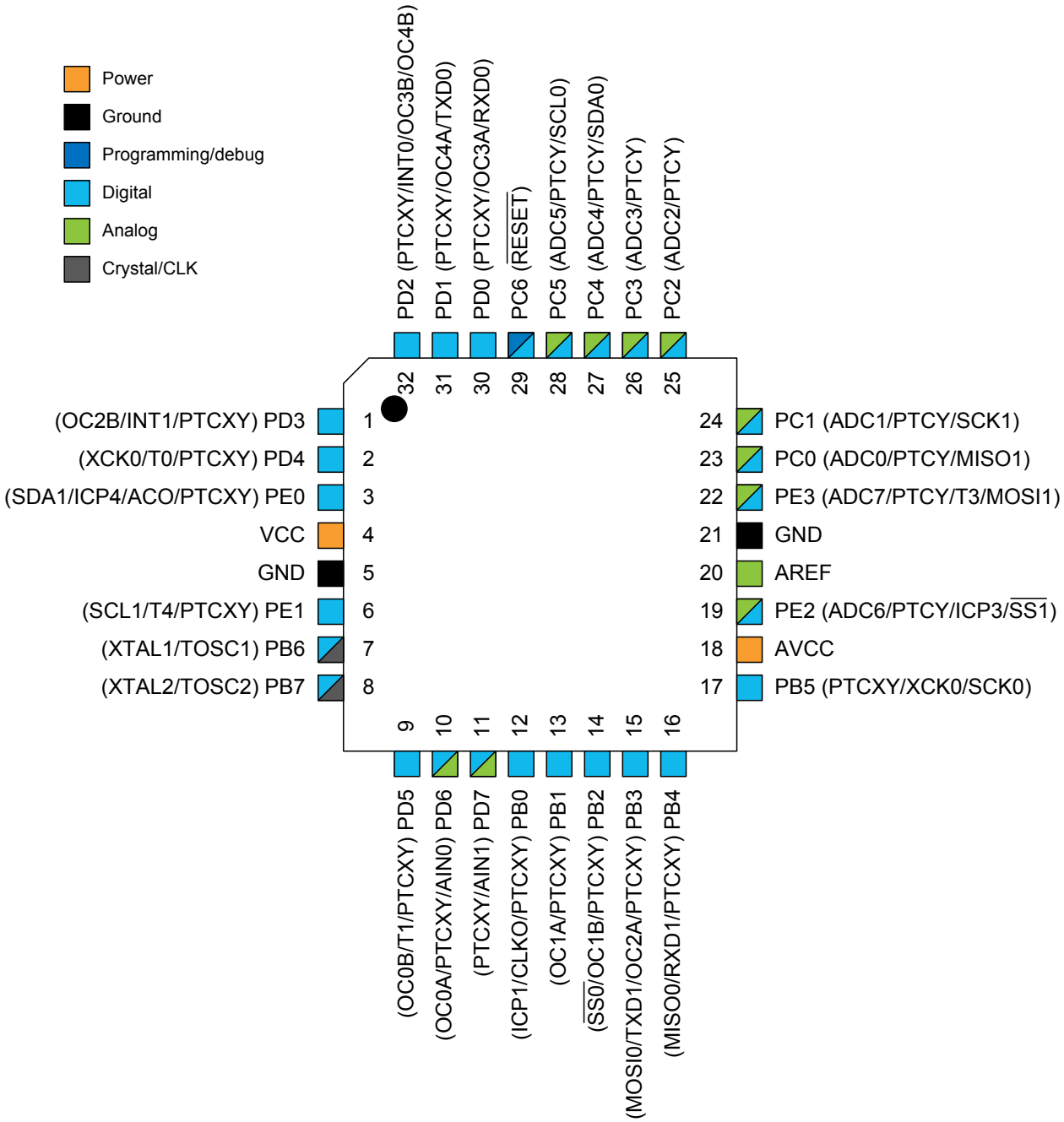
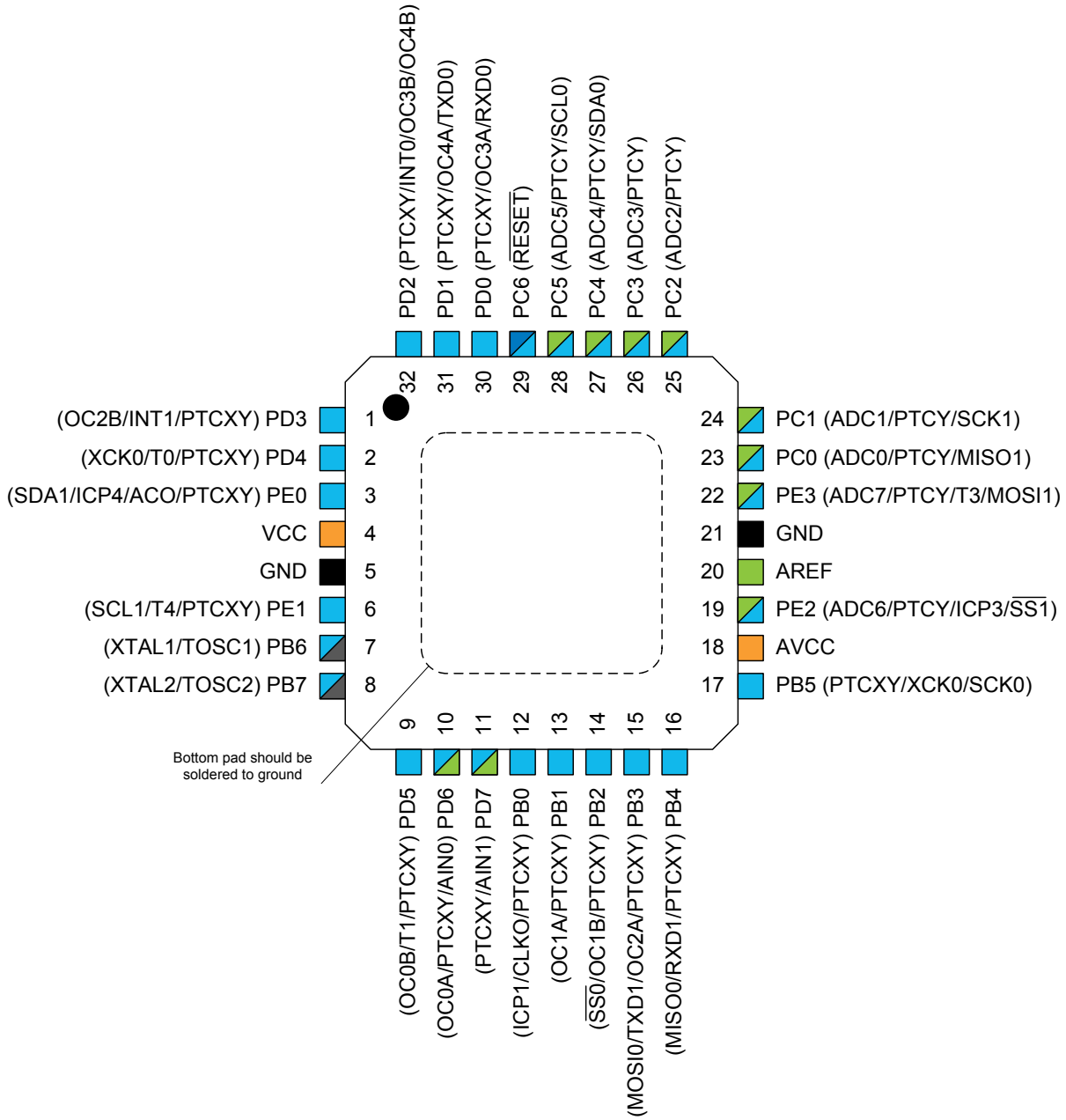


Figure 5-2 32 VQFN Pinout ATmega328PB



5.1. Pin Descriptions

5.1.1. VCC

Digital supply voltage.

5.1.2. GND

Ground.

5.1.3. Port B (PB[7:0]) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs,

Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB[7:6] is used as TOSC[2:1] input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

5.1.4. Port C (PC[5:0])

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC[5:0] output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.1.5. PC6/RESET

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated in #unique_14.

5.1.6. Port D (PD[7:0])

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.1.7. Port E (PE[3:0])

Port E is an 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.1.8. AV_{CC}

AV_{CC} is the supply voltage pin for the A/D Converter, PC[3:0], and PE[3:2]. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that PC[6:4] use digital supply voltage, V_{CC}.

5.1.9. AREF

AREF is the analog reference pin for the A/D Converter.

5.1.10. ADC[7:6] (TQFP and VFQFN Package Only)

In the TQFP and VFQFN package, ADC[7:6] serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

6. I/O Multiplexing

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 6-1 PORT Function Multiplexing

No	PAD	EXTINT	PCINT	ADC/AC	PTC X	PTC Y	OSC	T/C # 0	T/C # 1	USART	I2C	SPI
1	PD[3]	INT1	PCINT19		X3	Y11		OC2A				
2	PD[4]		PCINT20		X4	Y12		T0		XCK0		
3	PE[0]		PCINT24	ACO	X8	Y16			ICP4		SDA1	
4	VCC											
5	GND											
6	PE[1]		PCINT25		X9	Y17			TC4		SCL1	
7	PB[6]		PCINT6				XTAL1/TOSC1					
8	PB[7]		PCINT7				XTAL2/TOSC2					
9	PD[5]		PCINT21		X5	Y13		OC0B	T1			
10	PD[6]		PCINT22	AIN0	X6	Y14		OC0A				
11	PD[7]		PCINT23	AIN1	X7	Y15						
12	PB[0]		PCINT0		X10	Y18	CLKO	ICP1				
13	PB[1]		PCINT1		X11	Y19		OC1A				
14	PB[2]		PCINT2		X12	Y20		OC1B				$\overline{SS0}$
15	PB[3]		PCINT3		X13	Y21		OC2A		TXD1		MOSI0
16	PB[4]		PCINT4		X14	Y22				RXD1		MISO0
17	PB[5]		PCINT5		X15	Y23				XCK0		SCK0
18	AVCC											
19	PE[2]		PCINT26	ADC6		Y6		ICP3				$\overline{SS1}$
20	AREF											
21	GND											
22	PE[3]		PCINT27	ADC7		Y7		T3				MOSI1
23	PC[0]		PCINT8	ADC0		Y0						MISO1
24	PC[1]		PCINT9	ADC1		Y1						SCK1
25	PC[2]		PCINT10	ADC2		Y2						
26	PC[3]		PCINT11	ADC3		Y3						
27	PC[4]		PCINT12	ADC4		Y4					SDA0	
28	PC[5]		PCINT13	ADC5		Y5					SCL0	
29	PC[6]/$\overline{RESET}$		PCINT14									
30	PD[0]		PCINT16		X0	Y8		OC3A		RXD0		
31	PD[1]		PCINT17		X1	Y9			OC4A	TXD0		
32	PD[2]	INT0	PCINT18		X2	Y10		OC3B	OC4B			

7. Resources

A comprehensive set of development tools, application notes, and datasheets are available for download on http://www.atmel.com/avr.

8. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

9. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

10. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(0xFF)	Reserved	–	–	–	–	–	–	–	–
(0xFE)	Reserved	–	–	–	–	–	–	–	–
(0xFD)	Reserved	–	–	–	–	–	–	–	–
(0xFC)	Reserved	–	–	–	–	–	–	–	–
(0xFB)	Reserved	–	–	–	–	–	–	–	–
(0xFA)	Reserved	–	–	–	–	–	–	–	–
(0xF9)	Reserved	–	–	–	–	–	–	–	–
(0xF8)	Reserved	–	–	–	–	–	–	–	–
(0xF7)	Reserved	–	–	–	–	–	–	–	–
(0xF6)	Reserved	–	–	–	–	–	–	–	–
(0xF5)	Reserved	–	–	–	–	–	–	–	–
(0xF4)	Reserved	–	–	–	–	–	–	–	–
(0xF3)	Reserved	–	–	–	–	–	–	–	–
(0xF2)	Reserved	–	–	–	–	–	–	–	–
(0xF1)	Reserved	–	–	–	–	–	–	–	–
(0xF0)	Reserved	–	–	–	–	–	–	–	–
(0xEF)	Reserved	–	–	–	–	–	–	–	–
(0xEE)	Reserved	–	–	–	–	–	–	–	–
(0xED)	Reserved	–	–	–	–	–	–	–	–
(0xEC)	Reserved	–	–	–	–	–	–	–	–
(0xEB)	Reserved	–	–	–	–	–	–	–	–
(0xEA)	Reserved	–	–	–	–	–	–	–	–
(0xE9)	Reserved	–	–	–	–	–	–	–	–
(0xE8)	Reserved	–	–	–	–	–	–	–	–
(0xE7)	Reserved	–	–	–	–	–	–	–	–
(0xE6)	Reserved	–	–	–	–	–	–	–	–
(0xE5)	Reserved	–	–	–	–	–	–	–	–
(0xE4)	Reserved	–	–	–	–	–	–	–	–
(0xE3)	Reserved	–	–	–	–	–	–	–	–
(0xE2)	Reserved	–	–	–	–	–	–	–	–
(0xE1)	Reserved	–	–	–	–	–	–	–	–
(0xE0)	Reserved	–	–	–	–	–	–	–	–
(0xDF)	Reserved	–	–	–	–	–	–	–	–
(0xDE)	Reserved	–	–	–	–	–	–	–	–
(0xDD)	TWAMR1	TWAM16	TWAM15	TWAM14	TWAM13	TWAM12	TWAM11	TWAM10	–
(0xDC)	TWCR1	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
(0xDB)	TWDR1	TWD7	TWD6	TWD5	TWD4	TWD3	TWD2	TWD1	TWD0
(0xDA)	TWAR1	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE
(0xD9)	TWSR1	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0
(0xD8)	TWBR1	TWBR7	TWBR6	TWBR5	TWBR4	TWBR3	TWBR2	TWBR1	TWBR0
(0xD7)	Reserved	–	–	–	–	–	–	–	–
(0xD6)	Reserved	–	–	–	–	–	–	–	–
(0xD5)	Reserved	–	–	–	–	–	–	–	–
(0xD4)	Reserved	–	–	–	–	–	–	–	–

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(0xD3)	Reserved	–	–	–	–	–	–	–	–
(0xD2)	Reserved	–	–	–	–	–	–	–	–
(0xD1)	Reserved	–	–	–	–	–	–	–	–
(0xD0)	Reserved	–	–	–	–	–	–	–	–
(0xCF)	Reserved	–	–	–	–	–	–	–	–
(0xCE)	UDR1	USART I/O Data Register 1							
(0xCD)	UBBR1H	USART Baud Rate Register 1 High							
(0xCC)	UBBR1L	USART Baud Rate Register 1 Low							
(0xCB)	UCSR1D	RXIE	RXS	SFDE	–	–	–	–	–
(0xCA)	UCSR1C	UMSEL11	UMSEL10	UPM11	UPM10	USBS1	UCSZ11 / UDORD1	UCSZ10 / UCPHA1	UCPOL1
(0xC9)	UCSR1B	RXCIE1	TXCIE1	UDRIE0	RXEN1	TXEN1	UCSZ12	RXB80	TXB80
(0xC8)	UCSR1A	RXC1	TXC1	UDRE1	FE0	DOR1	UPE1	U2X1	MPCM1
(0xC7)	Reserved	–	–	–	–	–	–	–	–
(0xC6)	UDR0	USART I/O Data Register 0							
(0xC5)	UBBR0H	USART Baud Rate Register 0 High							
(0xC4)	UBBR0L	USART Baud Rate Register 0 Low							
(0xC3)	UCSR0D	RXSIE	RXS	SFDE	–	–	–	–	–
(0xC2)	UCSR0C	UMSEL01	UMSEL00	UPM01	UPM00	USBS0	UCSZ01 / UDORD0	UCSZ00 / UCPHA0	UCPOL0
(0xC1)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0
(0xBF)	Reserved	–	–	–	–	–	–	–	–
(0xBE)	Reserved	–	–	–	–	–	–	–	–
(0xBD)	TWAMR0	TWAM06	TWAM05	TWAM04	TWAM03	TWAM02	TWAM01	TWAM00	–
(0xBC)	TWCR0	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
(0xBB)	TWDR0	2-wire Serial Interface Data Register							
(0xBA)	TWAR0	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE
(0xB9)	TWSR0	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0
(0xB8)	TWBR0	2-wire Serial Interface Bit Rate Register							
(0xB7)	Reserved	–	–	–	–	–	–	–	
(0xB6)	ASSR	–	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB
(0xB5)	Reserved	–	–	–	–	–	–	–	–
(0xB4)	OCR2B	Timer/Counter2 Output Compare Register B							
(0xB3)	OCR2A	Timer/Counter2 Output Compare Register A							
(0xB2)	TCNT2	Timer/Counter2 (8-bit)							
(0xB1)	TCCR2B	FOC2A	FOC2B	–	–	WGM22	CS22	CS21	CS20
(0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	–	–	WGM21	WGM20
(0xAF)	Reserved	–	–	–	–	–	–	–	–
(0xAE)	SPDR1	SPI Data Register 1							
(0xAD)	SPSR1	SPIF1	WCOL1	–	–	–	–	–	SPI2X
(0xAC)	SPCR1	SPIE1	SPE1	DORD1	MSTR1	CPOL1	CPHA1	SPR1	SPR0
(0xAB)	OCR4BH	Timer/Counter4 - Output Compare Register B High Byte							
(0xAA)	OCR4BL	Timer/Counter4 - Output Compare Register B Low Byte							
(0xA9)	OCR4AH	Timer/Counter4 - Output Compare Register A High Byte							
(0xA8)	OCR4AL	Timer/Counter4 - Output Compare Register A Low Byte							
(0xA7)	ICR4H	Timer/Counter4 - Input Capture Register High Byte							

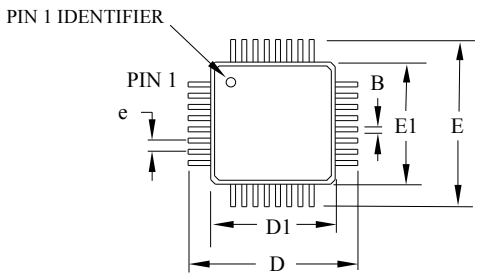
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(0xA6)	ICR4L	Timer/Counter4 - Input Capture Register Low Byte							
(0xA5)	Reserved	–	–	–	–	–	–	–	–
(0xA4)	Reserved	–	–	–	–	–	–	–	–
(0xA3)	Reserved	–	–	–	–	–	–	–	–
(0xA2)	TCCR4C	FOC4A	FOC4B	–	–	–	–	–	–
(0xA1)	TCCR4B	ICNC4	ICES4	–	WGM43	WGM42	CS42	CS41	CS40
(0xA0)	TCCR4A	COM4A1	COM4A0	COM4B1	COM4B0	–	–	WGM11	WGM10
(0x9F)	Reserved	–	–	–	–	–	–	–	–
(0x9E)	Reserved	–	–	–	–	–	–	–	–
(0x9D)	Reserved	–	–	–	–	–	–	–	–
(0x9C)	Reserved	–	–	–	–	–	–	–	–
(0x9B)	OCR3BH	Timer/Counter3 - Output Compare Register B High Byte							
(0x9A)	OCR3BL	Timer/Counter3 - Output Compare Register B Low Byte							
(0x99)	OCR3AH	Timer/Counter3 - Output Compare Register A High Byte							
(0x98)	OCR3AL	Timer/Counter3 - Output Compare Register A Low Byte							
(0x97)	ICR3H	Timer/Counter3 - Input Capture Register High Byte							
(0x96)	ICR3L	Timer/Counter3 - Input Capture Register Low Byte							
(0x95)	TCNT3H	Timer/Counter3 - Counter Register High Byte							
(0x94)	TCNT3L	Timer/Counter3 - Counter Register Low Byte							
(0x93)	Reserved	–	–	–	–	–	–	–	–
(0x92)	TCCR3C	FOC3A	FOC3B	–	–	–	–	–	–
(0x91)	TCCR3B	ICNC3	ICES3	–	WGM33	WGM12	CS32	CS31	CS30
(0x90)	TCCR3A	COM3A1	COM3A0	COM3B1	COM3B0	–	–	WGM31	WGM30
(0x8F)	Reserved	–	–	–	–	–	–	–	–
(0x8E)	Reserved	–	–	–	–	–	–	–	–
(0x8D)	Reserved	–	–	–	–	–	–	–	–
(0x8C)	Reserved	–	–	–	–	–	–	–	–
(0x8B)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte							
(0x8A)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte							
(0x89)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte							
(0x88)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte							
(0x87)	ICR1H	Timer/Counter1 - Input Capture Register High Byte							
(0x86)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte							
(0x85)	TCNT1H	Timer/Counter1 - Counter Register High Byte							
(0x84)	TCNT1L	Timer/Counter1 - Counter Register Low Byte							
(0x83)	Reserved	–	–	–	–	–	–	–	–
(0x82)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–
(0x81)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10
(0x7F)	DIDR1	–	–	–	–	–	–	AIN1D	AIN0D
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D
(0x7D)	Reserved	–	–	–	–	–	–	–	–
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0
(0x7B)	ADCSRB	–	ACME	–	–	–	ADTS2	ADTS1	ADTS0
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
(0x79)	ADCH	ADC Data Register High byte							
(0x78)	ADCL	ADC Data Register Low byte							

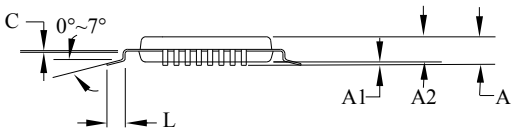
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(0x77)	Reserved	–	–	–	–	–	–	–	–
(0x76)	Reserved	–	–	–	–	–	–	–	–
(0x75)	Reserved	–	–	–	–	–	–	–	–
(0x74)	Reserved	–	–	–	–	–	–	–	–
(0x73)	Reserved	–	–	–	–	–	–	–	–
(0x72)	TIMSK4	–	–	–	–	–	–	–	–
(0x71)	TIMSK3	–	–	–	–	–	–	–	–
(0x70)	TIMSK2	–	–	–	–	–	OCIE2B	OCIE2A	TOIE2
(0x6F)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1
(0x6E)	TIMSK0	–	–	–	–	–	OCIE0B	OCIE0A	TOIE0
(0x6D)	PCMSK2	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0
(0x6A)	Reserved	–	–	–	–	–	–	–	–
(0x69)	EICRA	–	–	–	–	ISC11	ISC10	ISC01	ISC00
(0x68)	PCICR	–	–	–	–	–	PCIE2	PCIE1	PCIE0
(0x67)	Reserved	–	–	–	–	–	–	–	–
(0x66)	OSCCAL	Oscillator Calibration Register							
(0x65)	PRR1	–	–	PRTWI1	PRPTC	PRTIM4	PRSPI1	–	PRTIM3
(0x64)	PRR0	PRTWI	PRTIM2	PRTIM0	PRUSART1	PRTIM1	PRSPI	PRUSART0	PRADC
(0x63)	Reserved	–	–	–	–	–	–	–	–
(0x62)	CFDCSR(XFDCSR)	–	–	–	–	–	–	XFDIF	XFDIE
(0x61)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0
(0x60)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C
0x3E (0x5E)	SPH	–	–	–	–	–	SP10	SP9	SP8
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
0x3C (0x5C)	Reserved	–	–	–	–	–	–	–	–
0x3B (0x5B)	Reserved	–	–	–	–	–	–	–	–
0x3A (0x5A)	Reserved	–	–	–	–	–	–	–	–
0x39 (0x59)	Reserved	–	–	–	–	–	–	–	–
0x38 (0x58)	Reserved	–	–	–	–	–	–	–	–
0x37 (0x57)	SPMCSR	SPMIE	(RWWSB)4.	SIGRD	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN
0x36 (0x56)	Reserved	–	–	–	–	–	–	–	–
0x35 (0x55)	MCUCR	–	BODS	BODSE	PUD	–	–	IVSEL	IVCE
0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF
0x33 (0x53)	SMCR	–	–	–	–	SM2	SM1	SM0	SE
0x32 (0x52)	Reserved	–	–	–	–	–	–	–	–
0x31 (0x51)	Reserved	–	–	–	–	–	–	–	–
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0
0x2F (0x4F)	ACSR0	–	–	–	–	–	–	–	ACOE
0x2E (0x4E)	SPDR	SPI Data Register							
0x2D (0x4D)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
0x2B (0x4B)	GPIOR2	General Purpose I/O Register 2							
0x2A (0x4A)	GPIOR1	General Purpose I/O Register 1							
0x29 (0x49)	Reserved	–	–	–	–	–	–	–	–

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x28 (0x48)	OCR0B	Timer/Counter0 Output Compare Register B							
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare Register A							
0x26 (0x46)	TCNT0	Timer/Counter0 (8-bit)							
0x25 (0x45)	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00
0x24 (0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00
0x23 (0x43)	GTCCR	TSM	–	–	–	–	–	PSRASY	PSRSYNC
0x22 (0x42)	EEARH	EEPROM Address Register High Byte							
0x21 (0x41)	EEARL	EEPROM Address Register Low Byte							
0x20 (0x40)	EEDR	EEPROM Data Register							
0x1F (0x3F)	EECR	–	–	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE
0x1E (0x3E)	GPIOR0	General Purpose I/O Register 0							
0x1D (0x3D)	EIMSK	–	–	–	–	–	–	INT1	INT0
0x1C (0x3C)	EIFR	–	–	–	–	–	–	INTF1	INTF0
0x1B (0x3B)	PCIFR	–	–	–	–	PCIF3	PCIF2	PCIF1	PCIF0
0x1A (0x3A)	Reserved	–	–	–	–	–	–	–	–
0x19 (0x39)	TIFR4	–	–	ICF4	–	–	OCF4B	OCF4A	TOV4
0x18 (0x38)	TIFR3	–	–	ICF3	–	–	OCF3B	OCF3A	TOV3
0x17 (0x37)	TIFR2	–	–	–	–	–	OCF2B	OCF2A	TOV2
0x16 (0x36)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1
0x15 (0x35)	TIFR0	–	–	–	–	–	OCF0B	OCF0A	TOV0
0x14 (0x34)	PTIFR	–	–	–	–	–	–	–	–
0x13 (0x33)	Reserved	–	–	–	–	–	–	–	–
0x12 (0x32)	Reserved	–	–	–	–	–	–	–	–
0x11 (0x31)	Reserved	–	–	–	–	–	–	–	–
0x10 (0x30)	Reserved	–	–	–	–	–	–	–	–
0x0F (0x2F)	Reserved	–	–	–	–	–	–	–	–
0x0E (0x2E)	PORTE	–	–	–	–	PORTE3	PORTE2	PORTE1	PORTE0
0x0D (0x2D)	DDRE	–	–	–	–	DDRE3	DDRE2	DDRE1	DDRE0
0x0C (0x2C)	PINE	–	–	–	–	PINE3	PINE2	PINE1	PINE0
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
0x08 (0x28)	PORTC	–	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0
0x07 (0x27)	DDRC	–	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
0x06 (0x26)	PINC	–	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0
0x02 (0x22)	Reserved	–	–	–	–	–	–	–	–
0x01 (0x21)	Reserved	–	–	–	–	–	–	–	–
0x0 (0x20)	Reserved	–	–	–	–	–	–	–	–

11. Packaging Information

11.1. 32A





COMMON DIMENSIONS
(Unit of measure = mm)

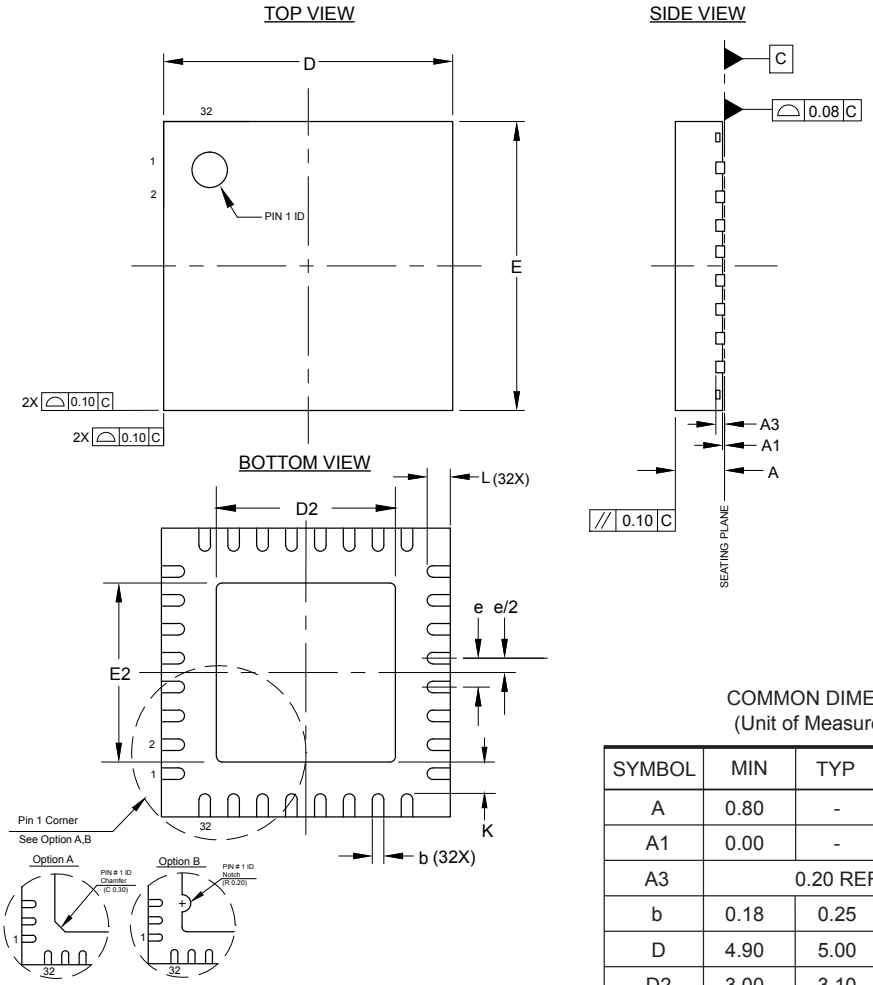
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

	TITLE	DRAWING NO.	REV.
Atmel	**32A,** 32-lead, 7 x 7mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)	32A	C

11.2. 32MS1



NOTE:

1. Refer to JEDEC Drawing MO-220, Variation VHHD-2 (Figure 1/Saw Singulation)
2. Dimension “b” applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimensions should not be measured in that radius area.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.80	-	0.90	
A1	0.00	-	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	2
D	4.90	5.00	5.10	
D2	3.00	3.10	3.20	
E	4.90	5.00	5.10	
E2	3.00	3.10	3.20	
e	-	0.50	-	
L	0.30	0.40	0.50	
K	0.20	-	-	

12/4/13

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 32MS1, 32-pad 5.0x5.0x0.9 mm Body, 0.50mm pitch, 3.1x3.1 mm Exposed pad, Saw Singulated Thermally Enhanced Plastic Very-thin Fine pitch, Quad Flat No Lead package (VFQFN)	GPC ZMF	DRAWING NO. 32MS1	REV. A

12. Errata

12.1. Rev. A

No known Errata.

12.2. Rev. B

Description:

If Chip Erase is performed at low supply voltage (VCC<3V), a flash read performed immediately after the chip erase (within 500ms) may show wrong results.

Workaround:

If chip erase is executed at a low voltage, wait for 500ms before reading the flash contents.

12.3. Rev. C

No known Errata.

13. Revision History

Doc Rev.	Date	Comments
42397C	10/2015	• Features : Added Unique Serial ID. Updated Power-down, Power save and removed the related note • Updated the Block Diagram on page 7 • Updated the Pin Configurations on page 8 • Removed the Electrical Specifications from the Configuration Summary • Updated the I/O Multiplexing section • Removed Capacitive Touch Sensing section • Updated the Low Power Crystal Oscillator Operating Modes and associated notes • Updated 128kHz Internal Oscillator section • Updated Operations section in CFD - Clock Failure Detection mechanism • Updated Reset and Interrupt Vectors in ATmega328PBB • Updated Alternate Port Function section • Removed the note below Input Capture Unit Block Diagram for TCn • Updated Figure Compare Match Output Unit, Schematic • Updated Figure Output Compare Unit, Block Diagram • Updated Figure Output Compare Modulator, Schematic • Updated Figure Output Compare Modulator, Timing Diagram • Updated Input Channel Selection • Updated Signature Row Addressing
42397B	09/2015	• Revised the Pin Diagram • Included new registers for Timer/Counter 3 and 4 • Updated Register Summary
42397A	07/2015	Initial document release.

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**