Laurel Electronics Co., Ltd.

OLED Module Specification

Model No.: LEG128642-W56

Table of Contents

1. BASIC SPECIFICATIONS ····· 2
2. ABSOLUTE MAXIMUM RATINGS ····· 7
3. OPTICAL & ELECTRICAL CHARACTERISTICS ····· 7
4. INITIALIZATION AND POWER OFF ····· 14
5. DIMENSIONAL OUTLINE ····· 15
6. PRECAUTIONS FOR USE OF OLED MODULES ····· 16

RECORD OF REVISION

Rev.	Date	Page	Item	Description
0.1	2019/09/12	-	-	New release

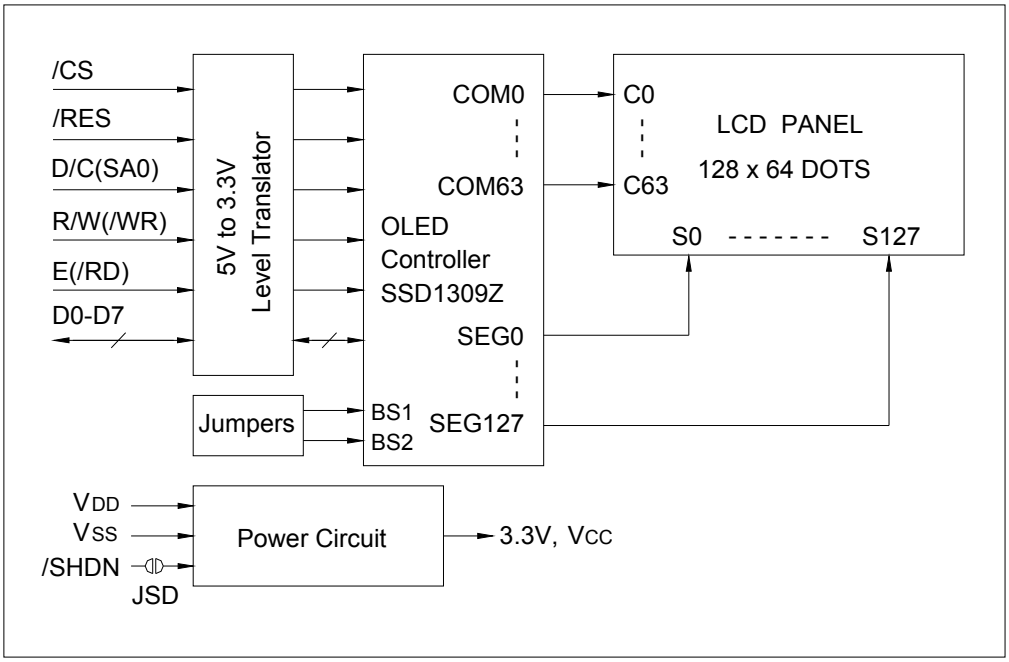
1. BASIC SPECIFICATIONS

1.1 Features

Item	Specifications	Unit
Screen Size	2.42 (Diagonal)	inch
Display Format	128 x 64	dot
OLED Type	Passive matrix	-
Display Color	White characters on black background	-
Driving Method	1/64 duty	-
Viewing Direction	Free	-
Outline Dimension (WxHxT)	75.0 x 52.7 x 8.0	mm
Viewing Area (WxH)	57.0 x 29.5	mm
Active Area (WxH)	55.01 x 27.49	mm
Dot Pitch (WxH)	0.43 x 0.43	mm
Dot Size (WxH)	0.4 x 0.4	mm
Weight	24	g
Controller	SSD1309Z	-
Interface	8-bit 6800/8080 parallel, 4-wire SPI or I^2C	-
Power Supply (V_{DD})	3.3 to 5.5	V

Note: Please refer to SSD1309 datasheet for details

1.2 Block Diagram



1.3 CN1/CN2 Terminal Functions (8-bit 6800 MPU interface)

Pin No.	Symbol	Level	Function
1	VDD	3.3V to 5.5V	Power supply
2	VSS	0V	Ground
3	NC or /SHDN	-	Jumper JSD open: No connection **<Default>** VCC converter is always turned on Jumper JSD close: Shutdown input for VCC voltage converter /SHDN= "H": VCC converter is turned on /SHDN= "L": VCC converter is turned off
4	D0	H/L	Bi-directional data bus
5	D1	H/L	
6	D2	H/L	
7	D3	H/L	
8	D4	H/L	
9	D5	H/L	
10	D6	H/L	
11	D7	H/L	
12	/CS	L	Chip selection signal. Chip is enabled when /CS is "L".
13	NC	-	Keep this terminal open or connect it to VDD or VSS
14	/RES	L	Reset signal. Internal reset is executed when /RES is "L".
15	R/W	H/L	Read or write selection R/W="H": Read operation R/W="L": Write operation
16	D/C	H/L	Data or command selection D/C="H": D0 to D7 are display data D/C="L": D0 to D7 are command code
17	E	H, H→L	Enable signal. In read mode (R/W="H"), data appears at D0 to D7 when E is "H". In write mode (R/W="L"), data of D0 to D7 is latched at the falling edge of E.
18	NC	-	Keep this terminal open or connect it to VDD or VSS
19	NC	-	Keep this terminal open or connect it to VDD or VSS
20	NC	-	Keep this terminal open or connect it to VDD or VSS

1.4 CN1/CN2 Terminal Functions (8-bit 8080 MPU interface)

Pin No.	Symbol	Level	Function
1	VDD	3.3V to 5.5V	Power supply
2	VSS	0V	Ground
3	NC or /SHDN	-	Jumper JSD open: No connection **<Default>** VCC converter is always turned on Jumper JSD close: Shutdown input for VCC voltage converter /SHDN= "H": VCC converter is turned on /SHDN= "L": VCC converter is turned off
4	D0	H/L	Bi-directional data bus
5	D1	H/L	
6	D2	H/L	
7	D3	H/L	
8	D4	H/L	
9	D5	H/L	
10	D6	H/L	
11	D7	H/L	
12	/CS	L	Chip selection signal. Chip is enabled when /CS is "L".
13	NC	-	Keep this terminal open or connect it to VDD or VSS
14	/RES	L	Reset signal. Internal reset is executed when /RES is "L".
15	/WR	L	Write signal. Data is latched at the rising edge of /WR.
16	D/C	H/L	Data or command selection D/C="H": D0 to D7 are display data D/C="L": D0 to D7 are command code
17	/RD	L	Read signal. Data appears at D0 to D7 when /RD is "L".
18	NC	-	Keep this terminal open or connect it to VDD or VSS
19	NC	-	Keep this terminal open or connect it to VDD or VSS
20	NC	-	Keep this terminal open or connect it to VDD or VSS

1.5 CN1/CN2 Terminal Functions (4-wire SPI interface)

Pin No.	Symbol	Level	Function
1	VDD	3.3V to 5.5V	Power supply
2	VSS	0V	Ground
3	NC or /SHDN	-	Jumper JSD open: No connection **<Default>** VCC converter is always turned on Jumper JSD close: Shutdown input for VCC voltage converter /SHDN= "H": VCC converter is turned on /SHDN= "L": VCC converter is turned off
4	SCLK	L→H	Serial clock input. Data is shifted at the rising edge of SCLK.
5	SDIN	H/L	Serial data input
6 to 11	NC	-	Keep these terminals open or connect them to VDD
12	/CS	L	Chip selection signal. Chip is enabled when /CS is "L".
13	NC	-	Keep this terminal open or connect it to VDD or VSS
14	/RES	L	Reset signal. Internal reset is executed when /RES is "L".
15	NC	-	Keep this terminal open or connect it to VDD
16	D/C	H/L	Data or command selection D/C="H": D0 to D7 are display data D/C="L": D0 to D7 are command code
17	NC	-	Keep this terminal open or connect it to VDD
18 to 20	NC	-	Keep these terminals open or connect them to VDD or VSS

Note: 4-wire SPI interface mode supports write operation only. Read operation is not supported.

1.6 CN1/CN2 Terminal Functions (I^2C interface)

Pin No.	Symbol	Level	Function
1	VDD	3.3V to 5.5V	Power supply
2	VSS	0V	Ground
3	NC or /SHDN	-	Jumper JSD open: No connection **<Default>** VCC converter is always turned on Jumper JSD close: Shutdown input for VCC voltage converter /SHDN= "H": VCC converter is turned on /SHDN= "L": VCC converter is turned off
4	SCL	H/L	I^2C bus serial clock input
5	SDAIN	H/L	I^2C bus serial data input
6	SDAOUT	L	Connect this terminal to VSS
7 to 12	NC	-	Keep these terminals open or connect them to VDD
13	NC	-	Keep this terminal open or connect it to VDD or VSS
14	/RES	L	Reset signal. Internal reset is executed when /RES is "L".
15	NC	-	Keep this terminal open or connect it to VDD
16	SA0	H/L	I^2C slave address
17	NC	-	Keep this terminal open or connect it to VDD
18 to 20	NC	-	Keep these terminals open or connect them to VDD or VSS

Note: I^2C bus mode supports write operation only. Acknowledge bit check or read operation is not supported.

1.7 Set Interface Bus Mode by on Board Jumpers

The interface bus mode is determined by terminals BS[2:1]. The relationship of the jumper status, BS[2:1] level and interface bus mode is below.

Jumper Status (C=Close; O=Open)						BS[2:1] Level	Interface Bus Mode
J68	J80	JS	JCSG	JBS2	JBS1		
C	O	O	O	O	C	1 0	**8-bit 6800 <Default>**
O	C	O	O	O	O	1 1	8-bit 8080
O	O	C	O	C	C	0 0	4-wire SPI
O	O	C	C	C	O	0 1	I^2C

Note:
1. 4-wire SPI interface mode supports write operation only. Read operation is not supported.
2. I^2C bus mode supports write operation only. Acknowledge bit check or read operation is not supported.

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	-0.3	6.0	V
Input Voltage	V_I	-0.3	V_{DD} + 0.3	V
Operating Temperature	Topr	-40	70	°C
Storage Temperature	Tstg	-40	80	°C

Cautions: Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. OPTICAL & ELECTRICAL CHARACTERISTICS

3.1 Optical Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Brightness Note 1	Lbr		60	80	-	cd/m^2
Color Chromaticity (White)	CIEx	CIE 1931	0.25	0.29	0.33	
	CIEy	CIE 1931	0.27	0.31	0.35	
Contrast Ratio	Cr	Dark Room	10,000:1	-	-	
Life Time Note 2		80 cd/m^2	30,000	-	-	hour
		60 cd/m^2	50,000	-	-	hour

Note:

1. V_{DD} = 3.3V to 5.5V, 100% display area turned on, the contrast control register value = DFH.
2. The life time is defined as the brightness decreases to 50% initial brightness at Ta=25°C, 50% checkerboard. The life time at Ta=25°C is estimated at accelerated operation at high temperature conditions. Luminance of the active pixels will degrade faster than the inactive pixels. Using a screen saver or the Display OFF command can extend the life time of the OLED.

3.2 DC Characteristics (Ta=25°C)

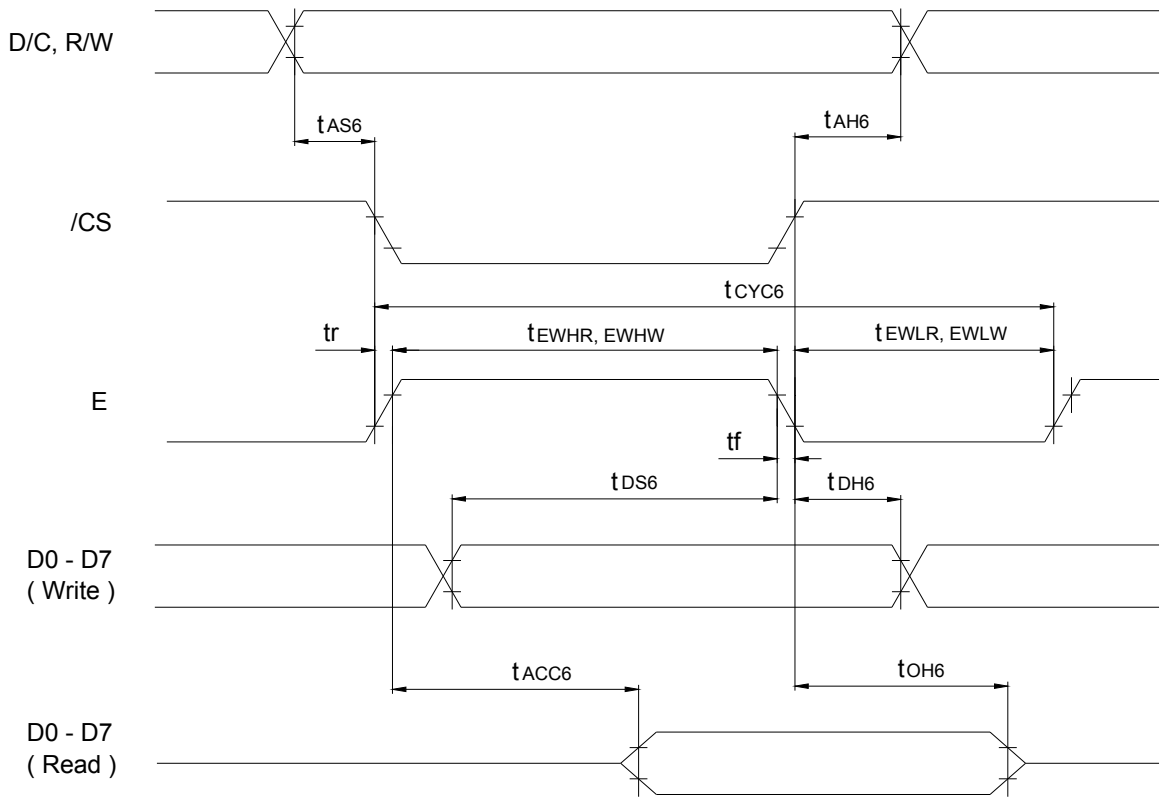
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		3.3	5.0	5.5	V
Input High Voltage	V_{IH}		2.0	-	V_{DD}	V
Input Low Voltage	V_{IL}		0	-	0.3V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = -0.1mA	V_{DD}-0.2	-	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OH} = 0.1mA	0	-	0.2	V
/SHDN High Voltage	$V_{IH\_/SHDN}$		1.0	-	V_{DD}	V
/SHDN Low Voltage	$V_{IL\_/SHDN}$		0	-	0.3	V
Supply Current	I_{DD}	V_{DD} = 5.0V Note 1	-	55.0	70.0	mA
		V_{DD} = 5.0V Note 2	-	90.0	110.0	mA
		V_{DD} = 5.0V Note 3	-	110.0	140.0	mA
		V_{DD} = 3.3V Note 1	-	85.0	105.0	mA
		V_{DD} = 3.3V Note 2	-	135.0	170.0	mA
		V_{DD} = 3.3V Note 3	-	180.0	225.0	mA
		V_{DD} = 3.3V to 5.5V Display off	-	3.0	5.0	mA

Note:

1. 30% display area turned on, the contrast register value = CFH
2. 50% display area turned on, the contrast register value = CFH
3. 100% display area turned on, the contrast register value = CFH

3.3 8-bit 6800 MPU Interface Timing Characteristics (3.3V to 5.5V, Ta=25°C)

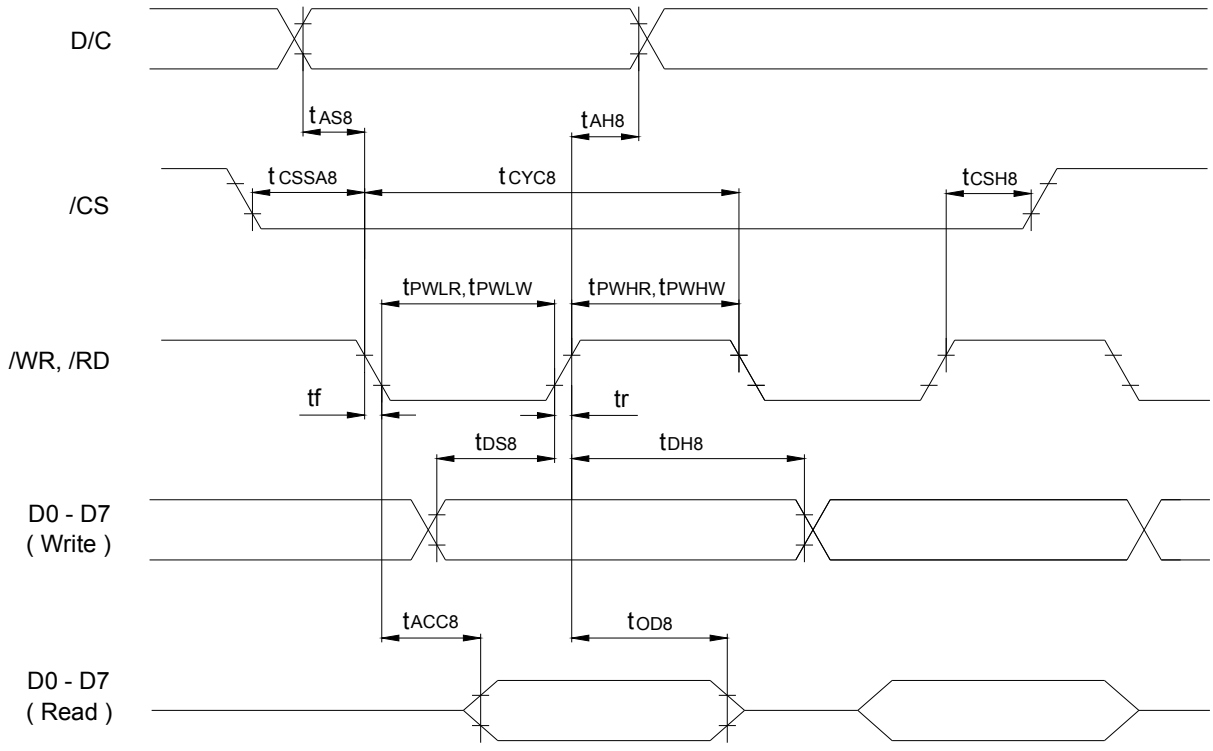
Item	Symbol	Min.	Max.	Unit
System Cycle Time	t_{CYC6}	300	-	ns
Address Setup Time	t_{AS6}	20	-	ns
Address Hold Time	t_{AH6}	0	-	ns
Data Setup Time	t_{DS6}	40	-	ns
Data Hold Time	t_{DH6}	20	-	ns
Data Output Disable Time	t_{OH6}	-	70	ns
Data Output Access Time	t_{ACC6}	-	140	ns
Enable High Pulse Width (Write)	t_{EWHW}	60	-	ns
Enable High Pulse Width (Read)	t_{EWHR}	120	-	ns
Enable Low Pulse Width (Write)	t_{EWLW}	60	-	ns
Enable Low Pulse Width (Read)	t_{EWLR}	60	-	ns
Rise Time	t_r	-	40	ns
Fall Time	t_f	-	40	ns



Bus Read/Write Timing (6800 Series MPU)

3.4 8-bit 8080 MPU Interface Timing Characteristics (3.3V to 5.5V, Ta=25°C)

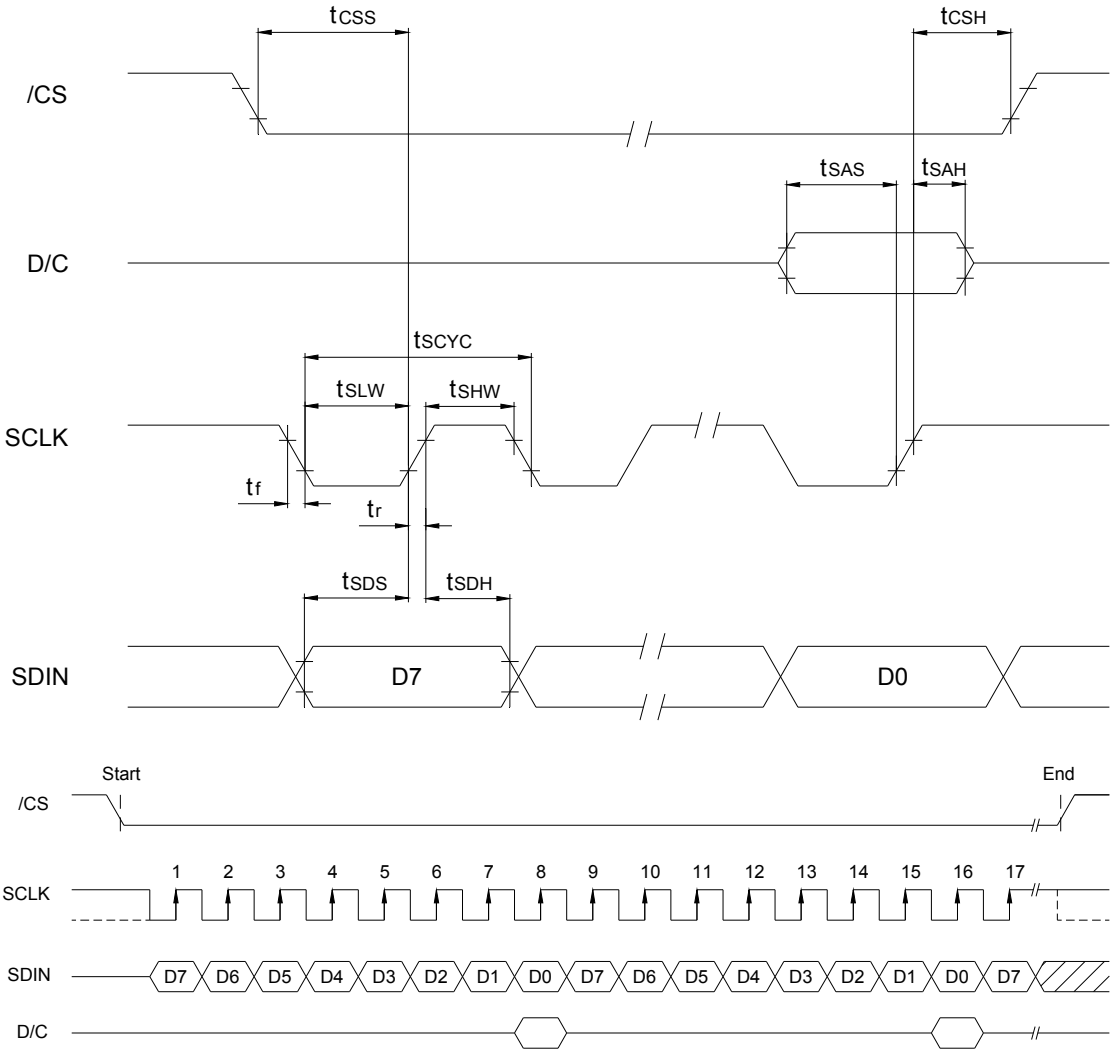
Item	Symbol	Min.	Max.	Unit
System Cycle Time	t_{CYC8}	300	-	ns
Chip Select Setup Time	t_{CSSA8}	0	-	ns
Chip Select Hold Time (read) (write)	t_{CSH8}	0 20	-	ns
Address Setup Time	t_{AS8}	20	-	ns
Address Hold Time	t_{AH8}	0	-	ns
Data Setup Time	t_{DS8}	40	-	ns
Data Hold Time	t_{DH8}	15	-	ns
Data Output Disable Time	t_{OD8}	-	70	ns
Read Access Time	t_{ACC8}	-	140	ns
Write Low Pulse Width	t_{PWLW}	60	-	ns
Read Low Pulse Width	t_{PWLR}	120	-	ns
Write High Pulse Width	t_{PWHW}	60	-	ns
Read High Pulse Width	t_{PWHR}	60	-	ns
Rise Time	t_r	-	40	ns
Fall Time	t_f	-	40	ns



Bus Read/Write Timing (8080 Series MPU)

3.5 4-wire SPI Interface Timing Characteristics (3.3V to 5.5V, Ta=25°C)

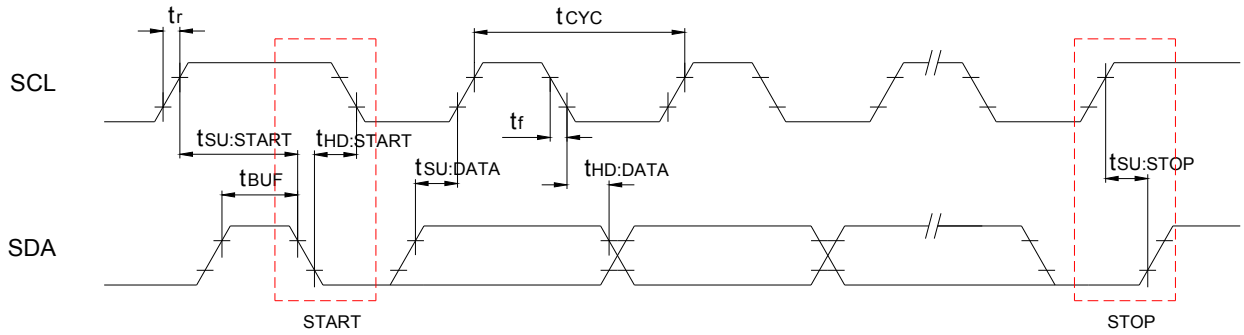
Item	Symbol	Min.	Max.	Unit
Serial Clock Cycle Time	t_{SCYC}	100	-	ns
Address Setup Time	t_{SAS}	15	-	ns
Address Hold Time	t_{SAH}	15	-	ns
Data Setup Time	t_{SDS}	15	-	ns
Data Hold Time	t_{SDH}	15	-	ns
Chip Select Setup Time	t_{CSS}	20	-	ns
Chip Select Hold Time	t_{CSH}	50	-	ns
Serial Clock High Pulse Width	t_{SHW}	50	-	ns
Serial Clock Low Pulse Width	t_{SLW}	50	-	ns
Rise Time	t_r	-	40	ns
Fall Time	t_f	-	40	ns



4-wire SPI Interface Timing

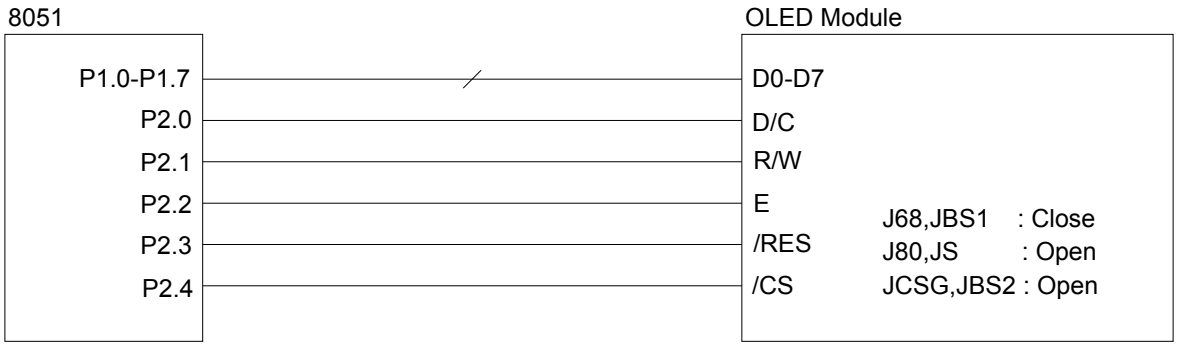
3.6 I²C Interface Timing Characteristics (3.3V to 5.5V, Ta=25°C)

Item	Symbol	Min.	Max.	Unit
SCL Clock Frequency	f_{SCL}	-	400	KHz
SCL Clock Cycle Time	t_{CYC}	2.5	-	μs
Data Setup Time	$t_{SU:DATA}$	100	-	ns
Data Hold Time	$t_{HD:DATA}$	300	-	ns
SCL, SDAIN Rise Time	t_r	-	300	ns
SCL, SDAIN Fall Time	t_f	-	300	ns
START Setup Time	$t_{SU:START}$	0.6		μs
START Hold Time	$t_{HD:START}$	0.6	-	μs
STOP Setup Time	$t_{SU:STOP}$	0.6	-	μs
Bus Free Time Between STOP and START Condition	t_{BUF}	1.3	-	μs

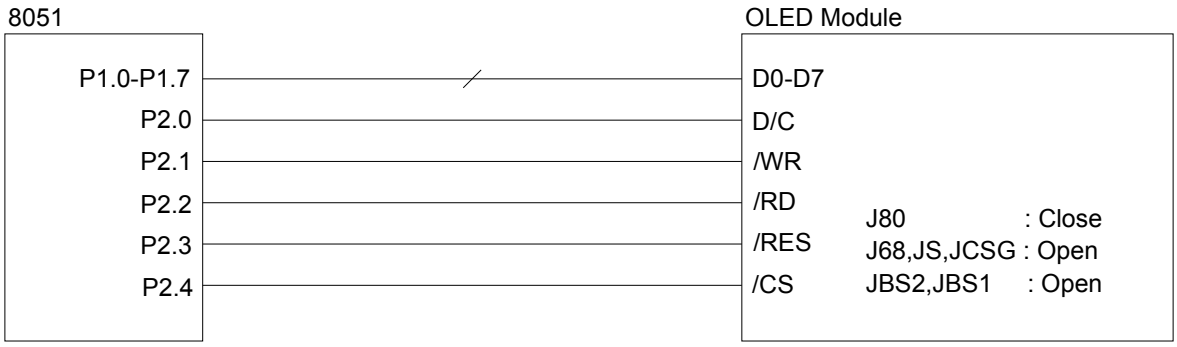


I²C Interface Timing

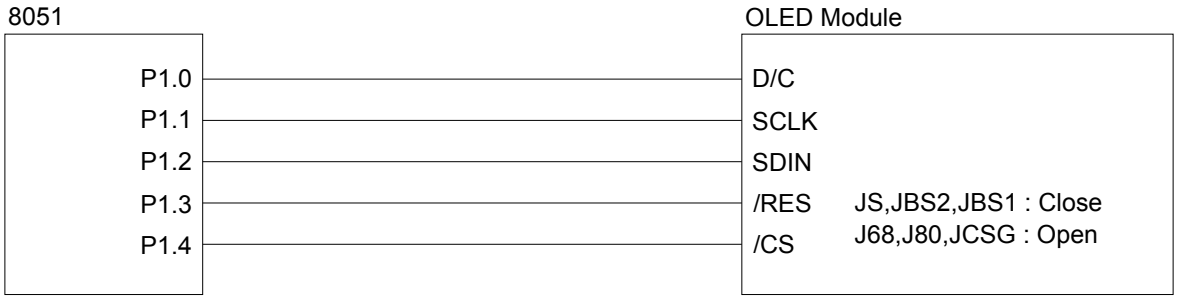
3.7 Connection with MPU



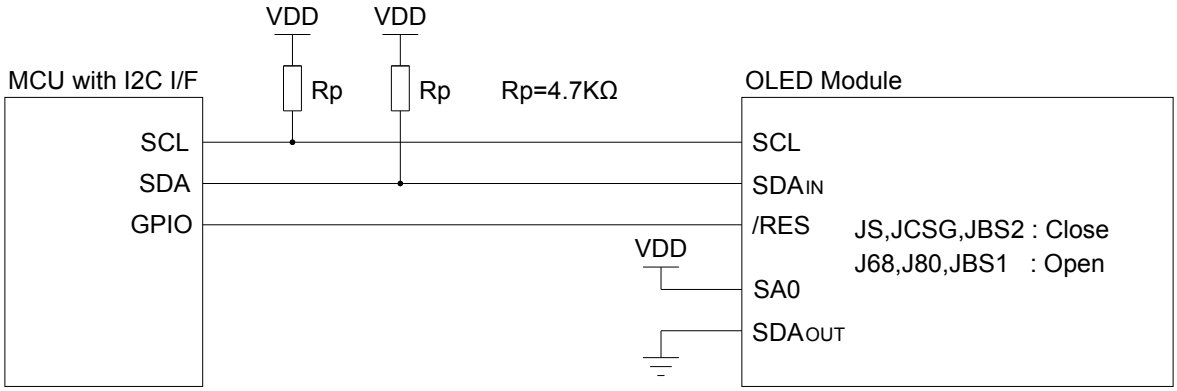
a. 6800 8-bit parallel interface



b. 8080 8-bit parallel interface



c. 4-wire SPI interface



d. I2C interface

4. INITIALIZATION AND POWER OFF

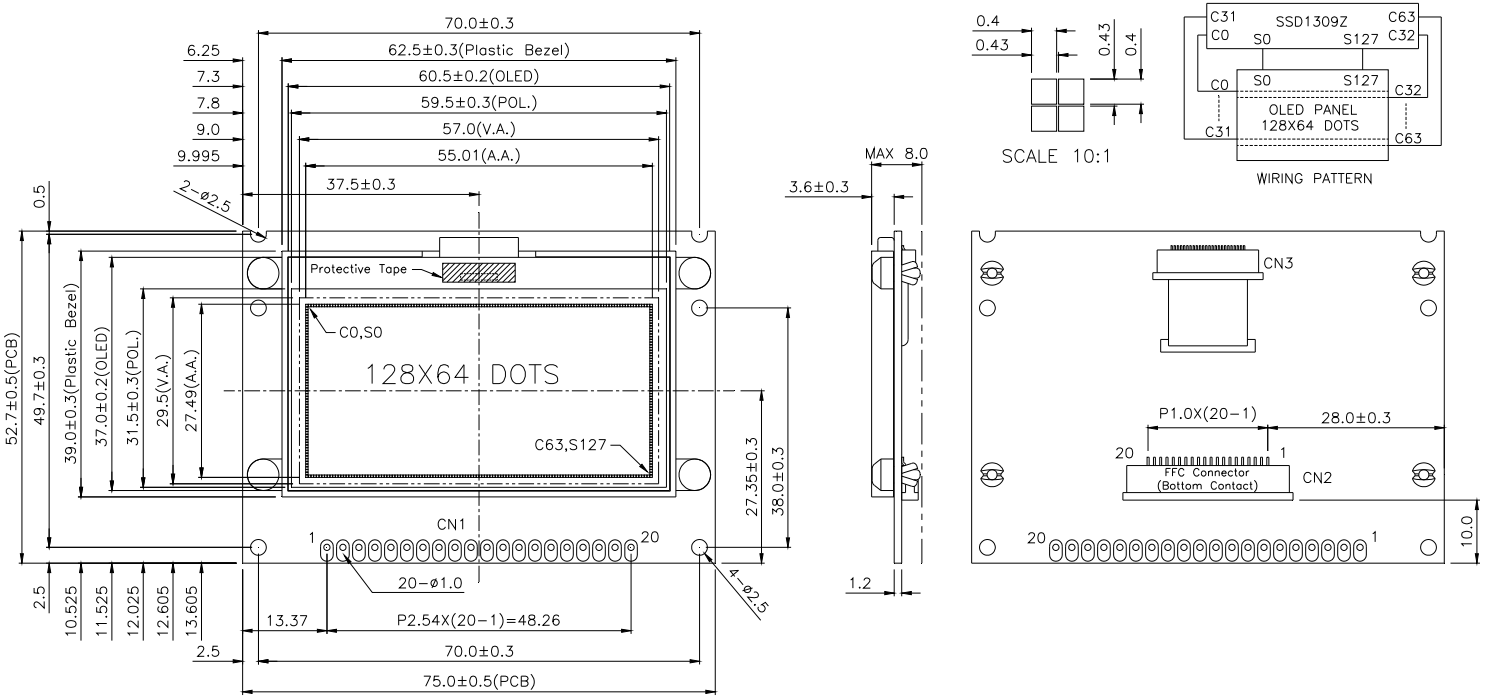
4.1 Power on Initialization Sequence

No.	Command	Description
1	Power on VDD	a. Power on VDD and wait for VDD stabilized b. Set /SHDN = "L" to shutdown VCC voltage converter (Skip this step when jumper JSD is open)
2	Reset	a. Set /RES = "L" b. Wait more than 100μs c. Set /RES = "H" d. Wait 1ms, and then start the initialization commands.
3	Set Command Lock: FDH, 12H	Unlock OLED driver IC interface from entering command
4	Set Display Off: AEH	Display off
5	Set Display Clock Divide Ratio/Oscillator Frequency: D5H, 70H	Display clock/frequency = 70H
6	Set Multiplex Ratio: A8H, 3FH	Multiplex ratio = 1/64 duty
7	Set Display Offset: D3H, 00H	Display offset = 00H
8	Set Display Start Line: 40H	Display start Line = 0
9	Set Memory Addressing Mode: 20H, 02H	Set page addressing mode
10	Set Segment Re-Map: A0H	Column address 0 mapped to SEG0
11	Set COM Output Scan Direction: C0H	COM scan from COM0 to COM63
12	Set COM Pins Hardware Configuration: DAH, 12H	Alternative COM pin configuration Disable COM left/right re-map
13	Set Contrast Control: 81H, CFH	Set contrast level = CFH
14	Set Pre-Charge Period: D9H, 82H	Phase 1 = 2 display clocks Phase 2 = 8 display clocks
15	Set VCOMH Deselect Level: DBH, 34H	VCOMH deselect level = 0.78 x VCC
16	Set Entire Display On/Off: A4H	Display outputs according to the DDRAM contents
17	Set Inverse Display Off: A6H	Normal display
18	Clear Screen	Clear screen
19	Power up VCC	Set /SHDN = "H" to enable VCC voltage converter (Skip this step when jumper JSD is open)
20	Set Display On: AFH	Display on
21	End of initialization	Delay 100ms and start to send other commands

4.2 Power off Sequence

No.	Command	Description
1	Set Display Off: AEH	Display off
2	Power down VCC	Set /SHDN = "L" to shutdown VCC voltage converter (Skip this step when jumper JSD is open)
3	Power down VDD	Delay 100 ms and then power down VDD

5. DIMENSIONAL OUTLINE



CN1/CN2 (6800 8-BIT PARALLEL I/F MODE)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SYMBOL	V_{DD}	V_{SS}	NC(/SHDN)	D0	D1	D2	D3	D4	D5	D6	D7	/CS	NC	/RES	R/W	D/C	E	NC	NC	NC

CN1/CN2 (8080 8-BIT PARALLEL I/F MODE)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SYMBOL	V_{DD}	V_{SS}	NC(/SHDN)	D0	D1	D2	D3	D4	D5	D6	D7	/CS	NC	/RES	/WR	D/C	/RD	NC	NC	NC

CN1/CN2 (4-WIRE SPI I/F MODE)

PIN NO.	1	2	3	4	5	6-11	12	13	14	15	16	17	18	19	20
SYMBOL	V_{DD}	V_{SS}	NC(/SHDN)	SCLK	SDIN	NC	/CS	NC	/RES	NC	D/C	NC	NC	NC	NC

CN1/CN2 (I2C I/F MODE)

PIN NO.	1	2	3	4	5	6	7-13	14	15	16	17	18	19	20
SYMBOL	V_{DD}	V_{SS}	NC(/SHDN)	SCL	SDA_{IN}	SDA_{OUT}	NC	/RES	NC	SA0	NC	NC	NC	NC

DWN.	LYJ	TITLE	LCM OUTLINE DIMENSION		
CHK.	LY	PART NO.	LEG128642		
APPD.		DWG. NO.	LEG128642-WXA		
REV.	A	UNIT	mm	PROJECTION	
DATE	2019.07.23	SCALE	NTS	SHEET	1 OF 1

6. PRECAUTIONS FOR USE OF OLED MODULES

6.1 Handing Precautions

1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
2) If the display panel is damaged and the internal organic substance leaks out, be sure not to get any in your mouth. If the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
3) Do not apply excessive force on the surface of the display or the adjoining areas of the module since this may damage the cell structure.
4) The polarizer covering the surface of OLED module is soft and easily scratched. Please be careful when handling the OLED module.
5) If the surface of the OLED module becomes contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents.
   · Isopropyl alcohol
   · Ethyl alcohol
   Solvents other than those mentioned above may damage the polarizer. Especially, do not use the followings:
   · Water
   · Ketone
   · Aromatic Solvents
6) When mounting the OLED module make sure it is free of twisting, warping and distortion. Distortion has great influence upon the display quality. Be sure the outer case holding the OLED module has sufficient rigidity.
7) Do not forcibly pull or bend the FPC terminals, apply stress to driver IC and the surrounding molded sections.
8) Do not disassemble nor modify (enlarging or making extra holes, etc.) the OLED module.
9) NC terminals should be open.
10) If the logic circuit power is off, do not apply the input signals.
11) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
   · Be sure to ground the human body when handling the OLED module.
   · Tools required for assembly, such as soldering irons, must be properly grounded.
   · To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
   · The surface of the OLED module is covered with a protective film. Exercise care when peeling off this protective film since static electricity may be generated.

6.2 Storage Precautions

1) When storing the OLED modules, put them in static electricity preventive bags and avoid exposure to direct sunlight or to the light of fluorescent lamps and high temperature/high humidity. Store the OLED modules in the packaged state when they were shipped from the manufacturer.
2) Exercise care to minimize corrosion of the electrodes. Corrosion of the electrodes is accelerated by water droplets or a current flow in a high humidity environment.

6.3 Design Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for the OLED module. Damage may happen if these values are exceeded,
2) To prevent the occurrence of erroneous operation caused by noise, attention must be paid to

satisfy VIL, VIH specifications, including making the signal line cable as short as possible.

3) Pay sufficient attention to avoid occurrence of the mutual noise interference occurred by peripheral devices.
4) To cope with EMI, take necessary measures on the outputting side of equipment.
5) When fastening the OLED module, fasten the external plastic housing section or the PCB.

6.4 Others

1) When an OLED module operates for a long of time with fixed patterns, the display patterns may remain on the screen as ghost images and slight contrast deviation may occur. If the operation is interrupted and the display is left unused for a while, normal state can be restored. This phenomenon does not adversely affect the reliability of the OLED module.
2) To minimize the performance degradation resulting from destruction caused by static electricity, etc., exercise care to avoid touching the following sections when handling the module:
   · Pins and electrodes
   ·Pattern layouts such as the FPC
3) Although the OLED module store the operation state data by the commands and the indication data, excessive external noise can enter into the module and the internal status may be changed. It is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
4) We recommend users to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.
5) Request the qualified companies to handle industrial wastes when disposing of the OLED modules.